National & Kapodistrian University of Athens

Science School

Department of Physics & Department of Informatics and Telecommunications

MASTER THESIS

Credibility Analysis for On-Chip Delay Monitors in View of Transistor Variability

Author:
Christiana Kapatsori

Supervisor:
Prof. Dimitrios Soudris

Athens

March 26, 2015

National & Kapodistrian University of Athens

Department of Physics & Department of Informatics and Telecommunications

Submitted by Chritiana D. Kapatsori (2012506)

DEFENCE COMMITTEE AND FINAL READING APPROVALS

Thesis Title : Credibility Analysis for Delay Measurement Structures in View of Transistor Variability

Date of Final Oral Presentation : Thursday 19/02/2015

Dimitrios Soudris	Antonis Paschalis
Angela Arapoyanni	Christiana Kapatsori

Abstract

High reliability has come to be a necessity in today's circuits as, with the advances in performance and the downscale in CMOS technology, the damages by failures are increasing. This impacts on circuit's designing with the need to extensively test and simulate the systems and demand an even higher reliability profile.

As the technology tends to reach below deca-nanometre levels in sizing the embedded sensors that monitor the circuits and ensure their reliability, face the same constraints in sizing downscale and high quality. Nevertheless they also face Temperature, Voltage and Process variations that may interfere with their measurements. These factors are modelled as time-zero and dynamic variations and are described by models such as Random Telegraph Noise, Time-Dependent Dielectric Breakdown, Bias Temperature Instability, optical phenomenon etc. In spite of the sensors usefulness they are not usually presented with a credible reliability analysis of their performance under variations.

In this thesis two sensors are simulated under time-zero variations and a reliability analysis has been made. With the use of Spice simulation and tools written in C++ and Perl we have tested the sensors and extracted statistics on their resolution. The Interpolation Method has been the basis of the designs and the statistical analysis has been made to have an estimation on the yield of these circuits.

Keywords: Yield, time-zero variability, aging sensors, interpolation method, Time-to-Digital Converters, Spice simulation

Περίληψη

Στις μέρες μας η αξιοπιστία των ηλεκτρονικών κυκλωμάτων έχει αποκτήσει μεγάλη σημασία, λόγω των συνεχώς αυξανόμενων απαιτήσεων σε απόδοση και την ταυτόχρονη μείωση των διαστάσεων της τεχνολογίας. Αποτέλεσμα αυτής της τάσης στον σχεδιασμό κυκλωμάτων είναι η ανάγκη για εκτενείς δοκιμές και προσομοιώσεις του κάθε κυκλώματος και η παραγωγή ενός αξιόπιστου προφίλ του εκάστοτε συστήματος.

Καθώς η τεχνολογία τείνει σε διαστάσεις κάτω των δέκα νανομέτρων, οι ενσωματωμένοι αισθητήρες είναι αυτοί που εξασφαλίζουν την αξιοπιστία των συστημάτων μέσω των συνεχών μετρήσεων. Ταυτόχρονα όμως, αντιμετωπίζουν τους ίδιους περιορισμούς όσων αφορά το μέγεθος τους και την υψηλή απόδοση. Καλούνται επίσης να λειτουργήσουν σε περιβάλλοντα οπου αντιμετωπίζουν μεταβολές θερμοκρασίας, τάσης και λειτουργίας που δύναται να επηρεάσουν τις μετρήσεις τους. Αυτοί οι παράγοντες μοντελοποιούνται ως μεταβολές την στιγμή λειτουργίας μηδέν και ως δυναμικές μεταβολές μέσω γνωστών μοντέλων όπως Random Telegraph Noise, Time-Dependent Dielectric Breakdown, Bias Temperature Instability, οπτικά φαινόμενα κ.α. Παρότι οι αισθητήρες είναι απαραίτητοι δεν ακολουθούνται πάντα από μία παρουσίαση της αξιοπιστίας τους υπό συνθήκες μεταβλητότητας.

Σε αυτή την διπλωματική πραγματοποιείται η προσομοίωση δύο αισθητήρων υπό συνθήκες μεταβολών την στιγμή λειτουργίας μηδέν, καθώς και η ανάλυση της αξιοπιστίας των μετρήσεών τους. Με την χρήση του εργαλείου Spice, καθως και μερικών εργαλείων γραμμένα σε C++και Perl προσομοιώθηκαν και εξήχθησαν στατιστικά αποτελέσματα όσων αφορά την ακρίβεια των μετρήσεων τους. Η μέθοδος της χρονικής παρεμβολής αποτέλεσε την βάση για τον σχεδιασμό των αισθητήρων και μέσω της στατιστικής ανάλυσης παρήχθησαν συμπεράσματα για την απόδοσή τους υπό συνθήκες μεταβλητότητας.

If at first the idea is not absurd, then there is no hope for it
–Albert Einstein

Acknowledgements

I would like to thank Professor Dimitrios Soudris, of National Technical University of Athens, for believing in me and being my advisor through the process of learning. His contribution was not only in a technical level but at guiding me in being a professional at my work and encouraging me in achieving more in the future.

This study would never have been accomplished without the contribution of Dimitrios Rodopoulos, PhD student and my supervisor. I would therefore like to thank him for his guidance throughout this thesis.

I would like to thank my parents and brother for their support in all the years of my studies, and last I thank my friends that we make this journey together.

Christiana Kapatsori

Athens, February 2015

Contents

List of Figures

Chapter 1

Introduction

With the gradual downscale in field-effect transistor (FET) devices, the phenomenon occurring are simulated by atomistic models [3]. This is drown by the necessity of having estimations on the yield of the devices and foresee the response of the circuit while operating under the conditions of Temperature or Voltage variations. By monitoring a circuit's response one can prevent sudden breakdowns or even manage the stress times, thus increasing the circuits life. Using the measurements of sensors, a circuit's designer can also reconfigure the system in order to achieve better performance and avoid system faults. When having a good approximation of the system's aging process or variability, one is able to manage it's workload and give a trustworthy profile of the it's reliability.

The gate oxide dielectric of transistors is the first to reach nanometre dimensions. This creates the need of accurate statistical models that simulate yield, while account time-zero and time-dependent variability [4]. Although having an accurate model will be the best case scenario, it does not solve the problem of aging as there are factors that affect the performance while the circuit works. Thus the use of sensors is a reasonable course of action.

Another aspect that monitoring can improve is building systems that achieve the best performance that they are capable of [5]. Designing more aggressively and customizing the circuits according to the application is today's tendency as Si-based technology nodes are reaching their limits. To be able to apply more strict clocking and voltage supply strategies

requires accuracy in the measurements of the response of the monitoring circuit. It is obvious that an embedded sensor faces the same time-zero and time-dependent variability as the circuit under investigation, as they are operating under similar conditions and suffer from the same semiconductor phenomena. In the above ways, the credibility of a sensor (i.e. its resolution and performance) may be partly at risk.

While the FET technology tends below deca-nanometer levels and the demands are of high quality, low cost manufacturing and low power consumption, the sensors that ensure these demands, should abide by similar constraints. In spite of their usefulness and their necessity, embedded Build-in Self-test(BIST) sensors sensors are not usually presented with an associated estimation of their credibility.

In this context, credibility can be expressed as the degree of accurate measurement that the sensor can make when it is subjected to variability effects such as time-zero variability. A credibility metric can be extracted by comparing responses with and without the semiconductor effect under investigation (e.g. time-zero variability). From this point of view, we can deduce that this issue needs further investigation and a simulation methodology is required to quantify the credibility of on-chip monitoring circuits. The current thesis project contributes towards this direction by (i) studying two different on-chip delay sensors under uniform time-zero variability and (ii) extracting their credibility metrics.

The main objective of this thesis is the development of an automated system that does a statistical analysis of on-chip monitoring circuits. A yield analysis has been implemented based on the linear interpolation method. The results are graphical representation of delay vs. a digital code. The delay is the time difference between the two input signals on the circuit. The output of the circuit is extracted from each cell and is converted to a digital code that represents whereas the two signals have yet met or not in the cell. This code consists of a number of digits same as the number of cells and, in overall, is the digital representation of the delay.

The yield curve is characterized by the equation $y = Ax + B$, where A is the slope of the line and B is the y-intercept. Thus, from the curves that result from the experiment for each sensor one can have an estimation of their response. The next step in the credibility metrics of the sensors is a disclaimer about six sigma confidence intervals of the mean sequences

[6]. By making a histogram from the data of A and B values after repetitive simulations we observe the deviation from the mean sequence and conclude on the variability of the sensors.

Finally the issues faced is the convergence of a Monte Carlo analysis and a further investigation of the variability of the p and n MOS transistors while varying the standard deviation of the time-zero variability parameters. These plots are discussed and the reliability profile of each sensor is viewed.

The structure of the thesis is as follows, Chapter 3 includes references in the related work in the field of yield phenomenon. It discuss other patterns that cause aging in systems and sensors, and the theoretical approach of the reliability issues is outlined. Chapter 4 presents the design of the two sensors and the use of the linear interpolation method. The Chapter 5 is the experiment validation section where it is described the experimental design used to extract the responses of the two sensors chosen to be implemented and gather the statistical data. The results of the experiments are presented in Chapter 6 and the conclusions and main finding of this thesis are briefly expounded in Chapter 7.

Chapter 2

Related Work

2.1 Introduction

According to Moore's law the number of the transistors that can be integrated in a circuit increases two times per year, an estimation which has proven right for some decades[7]. Nowadays, the concerns that technology has reached a dead end is still on but the reduction in feature sizes is in very low scaled technology. Also the expectations in accuracy and quality rise the difficulty of constructing a reliable Integrated Circuit(IC) into high levels.

The continuous downscale in feature sizes has brought challenges not only in the making of transistors with shorter gate length but also in the reliability of the today's ICs. With the reach of atomistic scale models, variation factors which are consistently occurring must be observed and modelled.

Process, voltage and temperature variations are reasons of aging and appearance of faults in ICs. The impact of each factor on a circuit differs according to the environment and the use of a circuit. Phenomena such as Negative Bias Instability (NBTI), Radiation Effects, Random Dopant Fluctuations etc. are some of the most dominant in topologies with increased area constraints and are going to be briefly discussed in this thesis.

In this Chapter, various causes of degradation will be presented. The main reasons of variation will be named and briefly explained in the advent of designing sensors that will face these degradation mechanisms. Pelgrom's law is also mentioned. Then the Interpolation

Method which is going to be followed is described and Time to Digital converters which are important to this method are explained. In the final Section of the Chapter a brief presentation of the theory of yield analysis is made.

2.2 Transistor Variability

As mentioned before another aspect of fault resulting in systems are the time-dependent variations which cause the decrease of a circuits lifetime. The most dominant concerns in aging faults are the Hot Carrier Injection phenomenon, Negative Bias Temperature Instability, and Time-dependent gate-oxide breakdown. Such phenomena are caused of stressing of the system but also because of high temperatures or high switching activity.

The most dominant phenomenon which cause variations and gradual device degradation is the issue of Negative Bias Instability. It has been investigated and addressed through many years since the decrease in the design technology, although a complete and reliably modes has not been developed yet. NBTI is relative to pMOS transistors whereas PBTI is to nMOS since it is referred to the gate voltage elevation due to the drain current[8].

BTI degradation refers to time-dependent instability in transistors and is a phenomenon that increases as the temperature rises. While performing a BTI stress test we can observe that the absolute drain current $I_{D_{sat}}$ and the transconductance of the MOS transistor are decreased due to an increase in temperature the threshold voltage V_T.[9]

Under negative V_{GS}, interface traps and positive oxide-fixed charge is generated, due to electrochemical reaction of holes and Si-H bonds at the $Si - SiO_2$ interface. Hence, V_{th_P} degradation depends not only on time, but also on the voltage and temperature history experienced by each p or nMOS. This shift in the threshold voltage decreases the drain current and impacts on the operation of the CMOS circuit.

Random Telegraph Noise (RTN) is an effect similar to BTI and causes oscillation in the threshold voltage in weak inversion[10]. RTN effect models the generation of descrete fluctuations in the conductance of the device due to an alteration at capture and emission of carriers at traps. Besides being a cause variation, RTN also is the source of low-frequency noise [11].

Two other critical mechanisms concerning reliability on CMOS technology, along with BTI and RTN, are the Hot Carrier Injection (HCI) and the Time Dependant Dielectric Breakdown (TDDB). Although it can be observed that these mechanisms are explained in a similar way, each one has a different impact and according to the operating conditions can be judged to be crucial.

As mentioned the BTI degradation is usual in sub-micro designs, whereas HCI can be observed in drivers with large loads and increased activity as they are exposed to repeated hot carrier stress and strong switching phases. In the Hot Carrier Injection phenomenon the threshold voltage varies as a function of drain voltage due to uneven trapped-carrier distribution near the drain. Thus traps can be found in the oxide when hot-carrier injection phenomenon happens.[12] A non-linear distribution of carriers trapped in the gate oxide is expected when simulating this process.

Hot Carrier limits the MOS transistors and is an impact caused by the need of increased electrical fields and new devices. But with the gate oxide of the transistors being reaching nanometre dimensions the systems are now introduced with another mechanism which questions their reliability, the Time-Dependent dielectric breakdown (TDDB). This degradation mechanism has historically been the limiting factor in choosing T_{ox}. The past pessimistic predictions of L_{min} can be directly attributed to a lack of understanding of the oxide breakdown limit due to long exposure to relatively low electric fields.

Due to atomistic level dimensions in nowadays devices, effects that interfere in the device's performance and cause variation are also such as Random Dopant Fluctuations (RDF) and Line-Edge Roughness (LER)[13]. RDF plays an important role in determining a circuits reliability as the gate's length has reached the deca-nanometer region. Dissimilarities in the pFET channel can be observed caused by RDF [14]. The imperfections during the process of photeresist removal or the photo count variations causes the LER phenomenon. When a system faces LER the I_{off}/I_{on} current ration increases, mostly in short channel circuits [15].

Optical Proximity Correction (OPC) is classified as photolithography technique in order to correct errors due to process effects in the masks [16]. This method is applied in the manufacturing process and makes partial changes on the image on the silicon wafer in

order to correct irregularities. This effect occurs as the light cannot make an accurate edge placement according to the initial design.

The variation effects described in this Chapter are considered while designing a circuit and are reasons for circuit's aging and gradual degradation. The standard deviation of the time-zero threshold voltage, caused by those variations can be expressed as follows, 2.1, [17] and can be represented by a Gaussian curve.

$$\sigma^2_{V_{th0}} \simeq \frac{t_{ox}\sqrt{N_A}}{A} \tag{2.1}$$

The voltage variations can be considered a sum of two factors, the as-fabricated, initial effects and time-dependent variations. In every device the threshold can be described by the equation2.2 where the first term is the time-zero variance and the term $\Delta V_{th}(t)$ is referring to the 'time-dependent degradation during circuit operation' [18].

$$V_{th}(t) = V_{th0} + \Delta V_{th}(t) \tag{2.2}$$

The BTI is, as mentioned, a dynamic factor whereas the factors of the RDF, TDDB etc. are initially considered as variation causes. When testing a circuit and extracting data for its reliability, it is a need to model all these existing factors, due to physical causes of variations. In this thesis is used only the time-zero variability model [13], to test the sensor's yield.

Pelgrom's rule establishes the relationship between the area of a FET and the threshold voltage, V_{th} [17]. It claims that the threshold voltage variation increases as the device's area is reduced and is inversely proportional to the square root of the device area. The relationship 2.3 referred as Pelgrom's law shows the correlation between the standard deviation of the threshold and the sizing of a FET.

$$\sigma_{V_{th}} = \frac{A_{VT}}{\sqrt{LW}} \tag{2.3}$$

In this thesis the Pelgrom's law is not set in the parameters of the circuit's design. Nevertheless it is taken under consideration when the results are discussed in the Conclusions

Chapter.

The advent of more sophisticated embedded systems that support reliance on deca-nanometer technologies for their fabrication, have brought reliability concerns to the fore-front. The focus of this thesis is investigating the credibility of delay monitors while in an environment with static variations.

2.3 Built-in self-test

An increasingly attractive solution in testing circuits is Built-in self-test (BIST) sensors. The purpose of BISTs is to extract statistics and parameters of the monitoring circuit which can characterize if it works like it is designed to. BIST sensors permit circuits to test themselves and offers high reliability, reduced complexity with no external equipment requirements [27]. The essence of BIST circuits is to internally generate test vectors and collect results, both purposes served by a single circuit.

BIST is a very common design technique to find in automotive applications, integrated circuits, medical devices, space application and in general machinery which may be unat-tended. Specifically in automotive applications it is of high importance to have circuits that are reliable and adaptable in order to face faults that may occur. This technique also contributes in having circuits with less test cost and better quality.

The general principle governing BIST is to initially generate test vectors and then verify the results. BIST are widely used because of the non-expensive implementation, it has the advantage of testing during operation and dynamic properties of the circuit can be tested at speed. Concurrent testing is also supported and can be used in different test levels.

The common strategies for testing are the Stored Patterns, the Exhaustive Testing, Pseudorandom Testing, Weighted Pseudorandom Testing and Pseudo exhaustive Testing. [28] Stored-pattern is an approach in which the test goals are set from the start and after the testing process the BIST detects the deviation from the goals. In the technique of Exhaustive Testing it is applied on the circuit a series of all possible inputs and all detectable faults are detected. It is often applied in complicated circuits but also in isolated small modules (PLAs).

Pseudorandom Testing differs as it applies test patterns with certain randomness. There is a deterministic order in the sequence of the test patterns and the faults are detected by the test length and the contents of the patterns. The method of Weighted Pseudorandom Testing also applies patterns with certain distribution (pseurorandom patterns) to face the random pattern resistant faults. Finally Pseudo exhaustive Testing partitions the system into smaller sub circuits and tests them exhaustively. This BIST design method requires extra effort in partitioning the circuit and provide them with the test patterns and test responses.

2.4 Time-to-Digital Converters

Time-interval digitization is well known technique for applications such as phase meters, aging sensors, etc [19]. By detecting the propagation delay on a circuit we can collect samples and information of great significance of the response of the circuit, thus Time-to-Digital Converters (TDCs) act as BISTs. The basis of the methodology is measuring the time-difference between two events occurring. In most implementations this is achieved by taking measurements of the time interval, meaning the time difference between the two rising edges of the inserted pulsed of the digital signals, or by measuring the duration of a pulse.

A fundamental unit used is the Delay Element (DE). There are many kinds of implementations of delay lines which consist of DEs [19]-[20], but many of them face the high power consumption and low resolution disadvantage.

The two DEs chosen in this thesis is firstly the inverter and then a custom design of a proposed sensor. The parameters that affect the response of these DEs are both their sizing and the number of the DE included in a delay line. The designer has the ability to choose whereas to adjust the inverter's transistor dimensions or to add an even number of inverter circuits and provide the design with a predictable time delay.

The Time Intervals (TI) produced by two lines of DE can be measured with various methods [21]. Dual interpolation method is preferred in this thesis and the TIs have been faced as follows : averaging and then analogue-to-digital converting. Due to the conversion

there is expected to have a linear dependence between the time delay and the digital code produced. The correlation is represented by a line with a intercept and a slope which are characteristic of the delay monitors.

The TDCs are widely used for extracting measurements for Time Delay Interpolation Method(TDIM). TDC units are very popular because they can have various uses, such as jitter measurement, time-of-flight measurements, etc.

Called to operate in low voltage supply environments, and being designed with minimum overhead but also high resolution, TDCs can be in architectures that utilize the delay difference between the logic gates[1], or with a passive on-chip voltage divider[22] and in architectures that provide improved resolution. These architectures are build by multiple stage interpolation lines and can be dynamic[23].

A TDC design can be attractive by adding a flip-flop or latch to the input of each delay line[24]. The result of this enhanced circuit is that on the rising edge of the clock, while on the stop phase, every delay line is been sampled. Hence, the start and the stop time difference can measure the signals switch. The advantage of this design is the use of simple cells with low overhead and also low power consumption as the power is only used while in conversion phase.

High resolution can be achieved in a TDC by following a method to analyse the extracted dataset from each Interpolation [25]. With the use of binary search for analysing the relative time delay between the signals and a Look Up Table for controlling the standard deviation of the circuit, an approximate resolution of 1.2ps can be reached. Another aspect yet to be inspected is the development of algorithms that correlate the expected results with the characteristics of the channels [26]

In overall, the use of TDCs is very attractive in many fields such as test applications, optical range-finding and on-chip self-testing topologies. Following the method of extracting digital codes from analogue responses of the circuit under test, has great advantages such as making the design adjustable, having the option of storing compressed information and even apply recovery methods.

2.5 Time-to-Digital Converter's Variability Analysis

To test the TDC's reliability is an issue of great importance as the circuits that gather information of the monitoring system, also face the same variability factors. This includes plotting a credibility curve under conditions of time-zero variability, then making a Monte Carlo analysis and finally plotting confidence intervals to observe the variations of the values of the mean (μ) and the standard deviation (σ).

To have an overall estimation of the response of the sensors, it is necessary to plot a credibility curve. This consists of the two variables A and B which represent the coefficients of the polynomial that produces the yield curve of each circuit. Each pair of A and B are drawn from a set of iteration of the simulation of the sensor, and after having a relatively credible normal distribution. By repeating the experiment many times we can achieve a good estimation not only on the response of the sensors but also on their reliability.

The TDC's response to a linear increase of the initial time delay between the two input signal is expected to be linear as well. Thus to every time delay attributes a specific digital code. This is represented by a line with equation $y = Ax + B$. Through the intercept and the slope of this line the characterization of the delay monitors is made. The two variables, the slope A and the intercept B, are set as shown in the qualitative figure 2.1 and suggest the monitor works ideally.

Due to variations though, this line may deviate from the expected. When the deviation is not perceptible the monitor can be considered reliable, but if the deviation is observable its response may be altered. The line represented as $y = A'x + B'$ is an acceptable response and shows that the circuit is under a variation factor but works properly. Limits such as upper and lower values in A and B (i.e. B_1 and B_2) suggest that if the line exceeds them the response can not be considered reliable.

By applying the same experiment and with the effect of time-zero variability, a statistical distribution is formed from the variation of the slope and the intercept. This forms a Gaussian distribution with a mean value and a standard deviation which characterise the variation from the reference values of A and B.

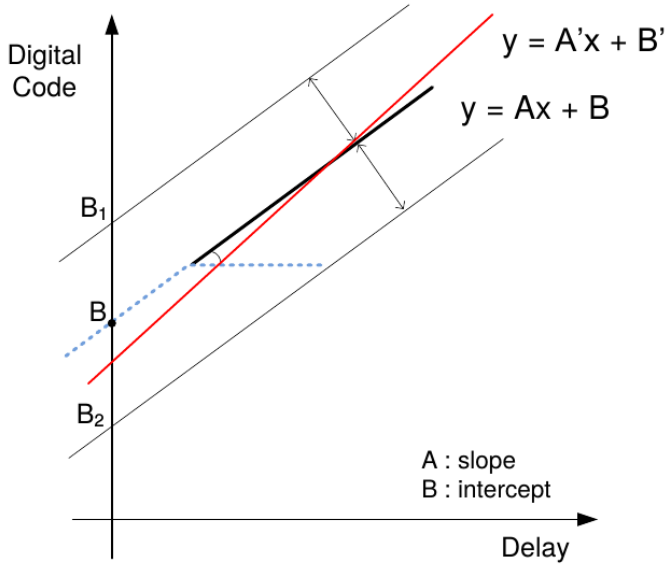


Figure 2.1: Time to Digital code conversion

The next step on the reliability analysis of a sensor is to visualize its credibility. It is of high necessity to know the upper and the lower bounds of each metric in order to have an error estimation. Using the selected confidence in 95% [6] we calculate and then plot the confidence limits of each set of results, i.e the μ and σ of A and B. It is expected for increased number of iterations the confidence to be increased.

A confidence interval represents the value of μ and σ of A and B extracted from the sensor, according to the number of iterations. It also includes the variations of these values on each metric, represented as a deviation. These are the error bounds from the mean values that complete the approximation on the behaviour of the circuit under investigation. As expected the confidence limits tend to expand as the observations tend to be less.

Another test designed in this thesis is to present the sensor to an environment with artificially inflating variability. By gathering statistics of the sensor's response to this conditions one can have a complete credibility analysis. Thus, since σ value is the metric which expresses the dispersion from the mean value in a normal curve, this also characterizes how the metrics can vary in each experiment. This is the parameter which is increased through our test.

The outcome of this set of simulations is an overall estimation on the diversion from the initial mean response, of the p and nMOS transistors respectively, since the standard

deviation of each differs. Through the metrics gathered from this test as the σ increases by a logarithmic step one can foretell the abnormal response of the sensor.

Chapter 3

Variability Analysis

3.1 Introduction

Variations in parameters in low scale technologies, poses a major challenge in circuit design. The process, voltage and temperature variations (P,V,T) are the main reasons that impact on the circuits response. Circuit failure prediction can be made by embedded sensors operating simultaneously with the system. The custom sensors are designed to extract measurements of variation and aging from the circuit that are embedded within.

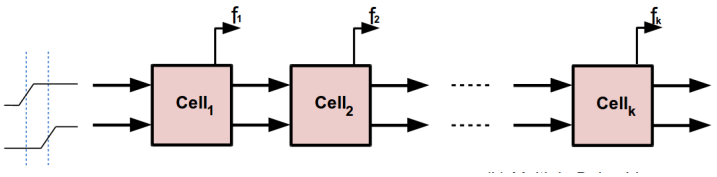
In this thesis we implement two sensors whose purpose is to measure delay. An open source version of the suit of SPICE programs was selected, the `ngspice`, which is a general-purpose circuit simulation framework[29]. Also the simulation of the effect of time-zero variability will be discussed and all the results expected from the experiment of the yield process on the aging sensors.

3.2 First Sensor

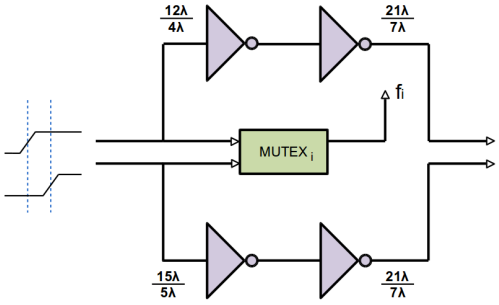
As mentioned before, Time Delay Interpolation Method (TDIM) constitutes the base to the design of the aging, on-Chip sensor that we implemented. According to TDIM we are able to measure relative delay through inserting signals in separate channels and then parsing the outputs. Each output of the sensor can be expressed as a digital value according to a threshold. If the two signals inserted in a cell of the sensor have met the output of this cell is the digit 1, otherwise it is 0.

This implementation classifies the sensor as a TDC. The number of the digits of the extracted code is proportionate to the number of cells 3.1a. If this number is increased the sensor outputs more accurate time-delay measurements as it detects in more cells if the signals have met. On the other hand, more accuracy adds more overhead, a factor which is very important as the sensor is embedded in the system. The choice of this proportion must be made according to the needs of the design.

For the design of the aging sensor, each individual cell constitutes of four inverters and a MUTEX [1]. The two inverter pairs have specific transistor sizing with proportions $12\lambda/4\lambda, 21\lambda/7\lambda$ and $15\lambda/5\lambda, 21\lambda/7\lambda$, as shown in the figure 3.1b.These fractions are multiplied with the sizing of the transistors which is predefined from the technology used.



(a) The Delay Line of the sensor



(b) A Delay Line Cell

A custom MUTEX has been designed in order to eliminate metastability 3.2. In our case metastability can be caused by two signals that are very close to each other, after the time-to-digital conversion. MUTEX's designed is based on the proposed circuit [1] that consists of two nand gates and four transistors.

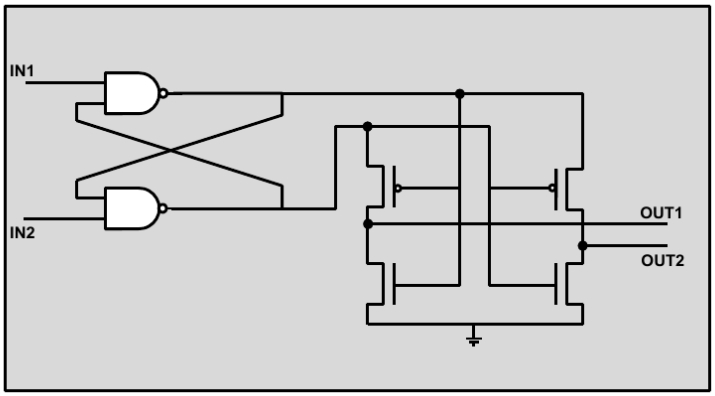


Figure 3.2: Custom MUTEX to filter metastability [1]

According to TDIM two pulses are inserted with time difference between them, and the faster signal is inserted in the longer delay element. This interval is translated to a digital code through the comparison between the two signals in each cell. Specifically the MUTEX placed after the delay lines in each cell has as input the pulses that travel through the delay lines. It's output characterize if the signal inserted in the longer delay element reached the signal that was inserted with a specific time delay, or not. When the signals have met the result of the comparison is a positive number, otherwise is a negative.

This is presented through the next figures where 3.3 is a representation of the two inputs of the sensor. The relative time difference between the two pulses is 0.3 nanoseconds. The first signal in 4.7 nanoseconds is inserted in the lower input of the cell, meaning the one with the greater sizing, whereas the pulse which is sent in 5 nanoseconds is inserted in the upper input.

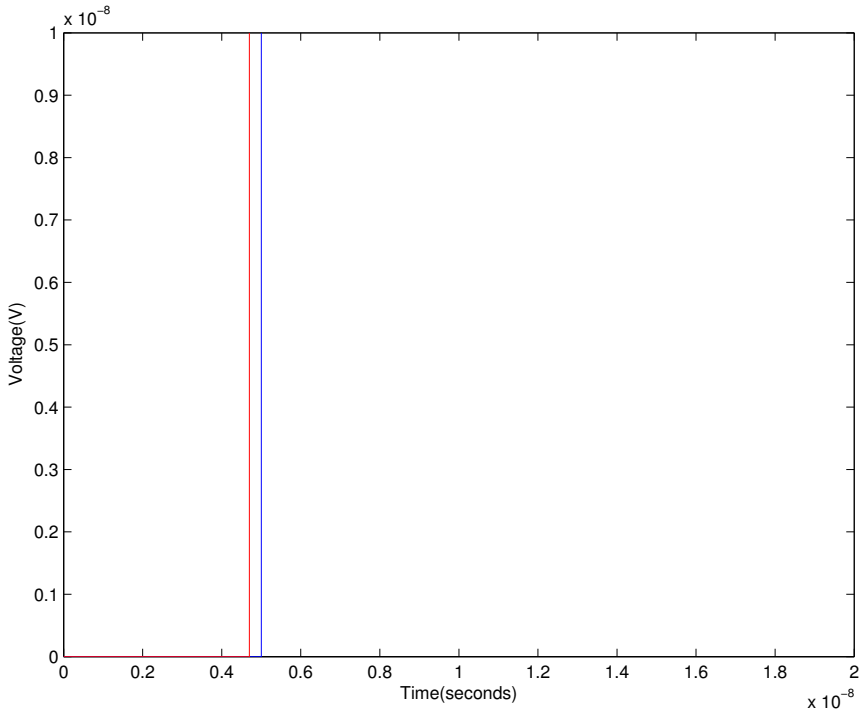


Figure 3.3: Input Pulses with time delay

Figures 3.4 and 3.5, show the response of the sensor after we have inserted the two pulses. The first one is the output of each inverter pair in every cell, thus ten inverter pairs. Each pair is shown with the same color. When the two waveforms meet then the MUTEX responds with elevated voltage, shown in figure 3.5. The two first waveforms seem to have small time difference which is the chosen initial delay. In the second pair this difference is decreasing, as in the third pair too and in the forth pair of measurements the two signal have already met. After that the difference shows to increase but the pulse that initially was inserted delayed now reaches the MUTEX first. This results in having the digit 1 as output and except from the three first digits which were 0 as the signals hadn't met all the rest express that the delayed signal has surpass the other. This increase in the time difference is physically explained as the delayed signal is inserted in the delay line with the small inverter sizing.

The time delay between the pulses is of the order of three tenths of nanosecond, thus the output of the TDC is the code 0001111111. As we can observe in the figure 3.4, that shows the output response of the delay elements, the digit 1 start to appear in the fourth pair of inverters.

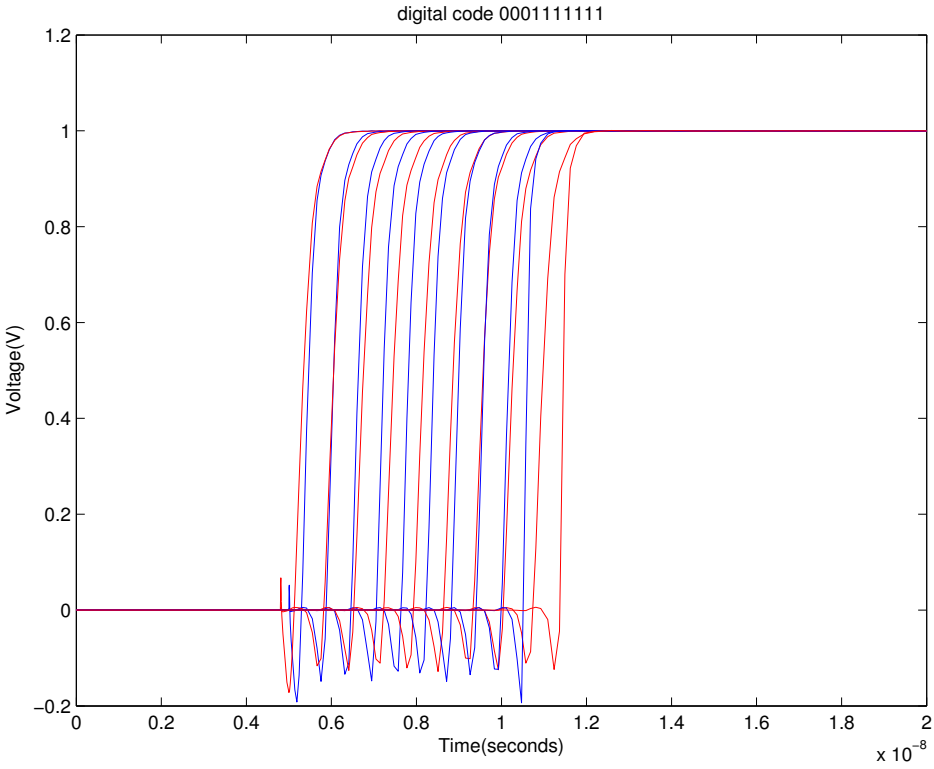


Figure 3.4: Response of Inverter Pairs, 1st sensor

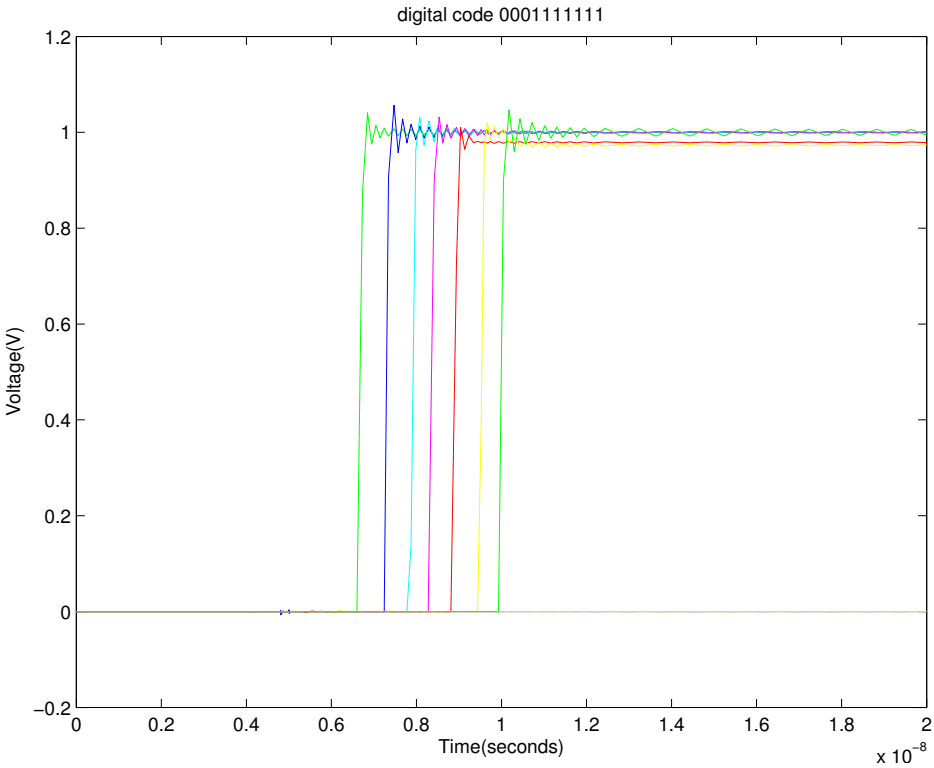


Figure 3.5: Digital Code Response of Sensor, 1st sensor

3.3 Second Sensor

The second circuit implemented is an aging sensor for Automotive Applications [2]. It is supported that this sensor is reliable and capable of performing in harsh environment with Process-Temperature variations and also low power supply. It's characteristic is that it can be programmable, a feature very positive for applications where the sensor is embedded and need to spare energy consumption. A drawback of the sensors topology is that the area overhead is significant, caused by the additional transistor in order to be programmable.

From the figure of the sensor 3.6 we can observe the extra transistors which are the input of a word, to make the sensor programmable. With this advantage the sensor can be turned OFF when ($PWD = 1$). When $PWD = 0$ the sensor is ON and the inverted clock signal $CLKN$ is created. This feature of the sensor is its advantage in lowering the power supply needed.

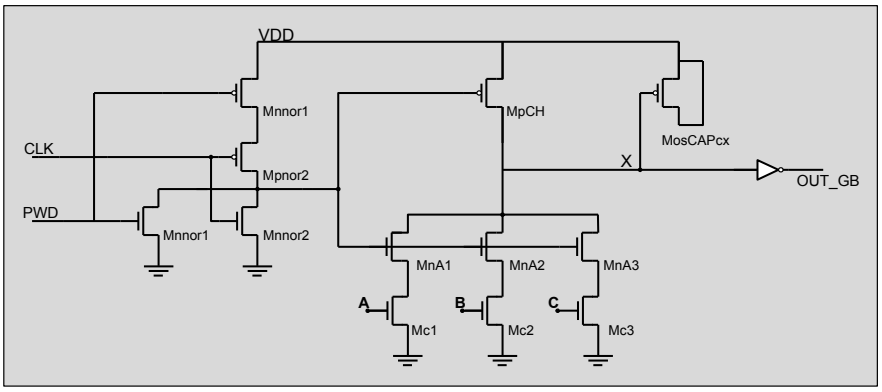


Figure 3.6: Programmable Aging Sensor for Automotive Applications[2]

The transistors M_{c1}, M_{c2} and M_{c3} from which the word is inserted (inputs A,B and C) will be ON when $CLKN = 1$ and will force the respective transistors M_{NA1}, M_{NA2} and M_{NA3}, either be ON or OFF. The response of the sensor thus depends not only on the input of the $CLKN$ but also on the word ABC inserted.This happens because, to have an output from the inverter there should be simultaneously the signal $CLKN$ on High and the $OUT_GB = 1$. The $OUT_GB = 1$ signal is directly connected with the inserted word. For example 'the lowest digital number as a word (001) leads to a minimum low pull-down current' [2], and the time for the discharging currents increases as the digital number does

so too.

For testing the sensor's aging resilience we implemented the circuit by following the Two Delay Interpolation Method (TDIM) as we did for the first circuit 3.1b. The result is a design with ten cells which include two delay lines with the sensor been the base of this design. The sizing is also the proposed from the first circuit and the rates are the $12\lambda/4\lambda, 21\lambda/7\lambda$ and $15\lambda/5\lambda, 21\lambda/7\lambda$ for each cell. Also the included MUTEX has the ability to filter metastability which takes as inputs the signal from the two delay lines 3.2.

To test the sensors responses to a pair of pulses inserted in the two delay lines, we simulated it's behaviour as shown in figure 3.7 and 3.8. The initial time difference is three tenths of nanosecond and the output digital code expected is 0001111111. Figure 3.7 shows the responses of each inverter pair in every cell and how the waveforms tend to meet, whereas figure 3.8 is the output of the ten cells that represent the digital code. The system designed with having as a cell the sensor for automotive applications now acts as a TDC. The resolution supported by this implementation is this of 10 measurements in a time difference of one nanosecond.

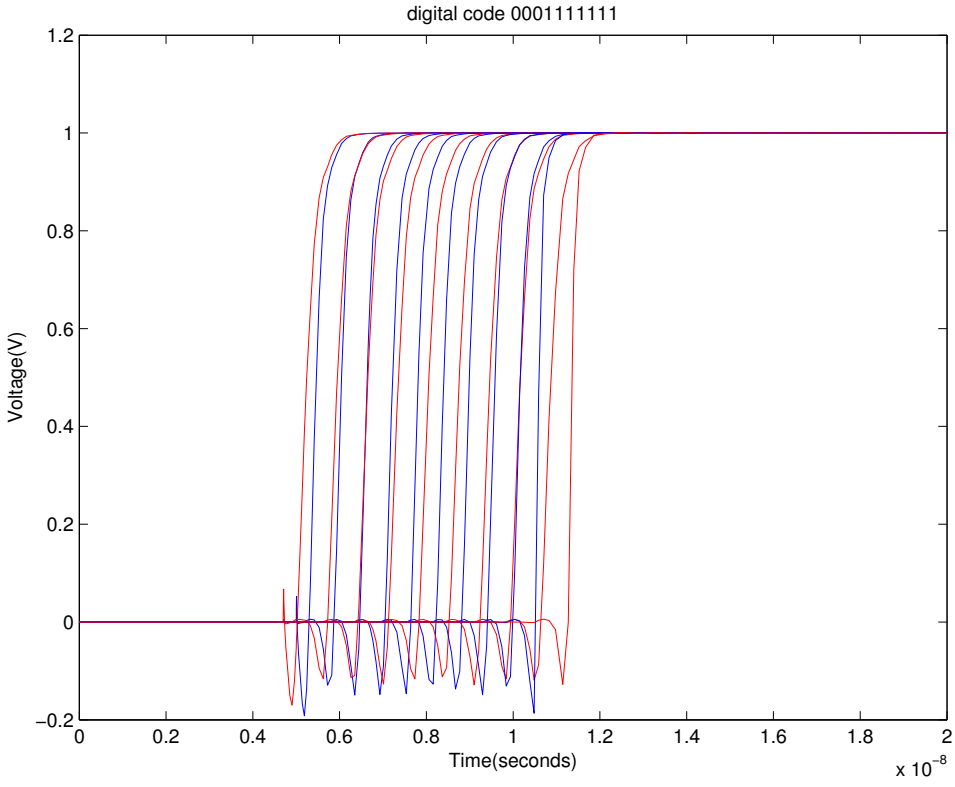


Figure 3.7: Response of Inverter Pairs, 2nd sensor

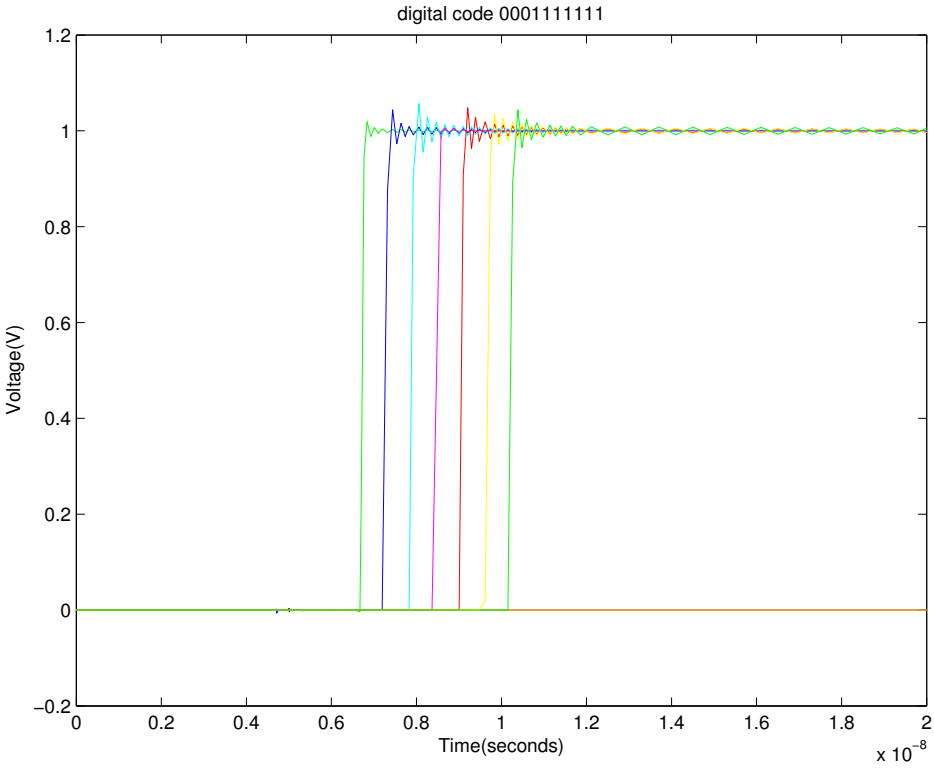


Figure 3.8: Digital Code Response of Sensor, 2nd sensor

Chapter 4

Credibility Metrics

4.1 Introduction

In integrated circuits there are many factors which can vary and many phenomenon that can occur. In our study we concentrate on process variations and especially we generate time-zero variations and observe the circuits response. This Chapter aims to built a background on the theory followed.

Firstly the circuits under investigation are designed and simulated in an open source tool, `ngspice`, which is a general-purpose circuit simulation framework, publicly available [29]. The results of each individual simulation are saved in an output file, produced automatically by the tool. This output file is in a non-readable format in order to have a graphical representation of the results. Thus a parsing tool has been designed in order to have an automated way of extracting information of the simulations.

As discussed in the previous Chapter the philosophy of testing a sensor for the aging process is based on Time Delay Interpolation Method (TDIM). According to this method, an initial time delay is been chosen for the two input signals that are inserted to the circuit. The system consists of the sensor under test, implemented with a specific sizing and repetition in order to construct two delay lines. The number of the cells can be adjustable and as many cells as the system has so many outputs it produces.

Following the TDIM method implies that we have to implement many cells to have a

digital code. The number of cells designed is selected to be ten, and so the digital code exists of ten digits simulating the initial time delay. This digital code changes depending on the time delay between the two test pulses. When the time-zero variability phenomenon occurs the circuit changes it's response and it is expected to have different digital output.

Each output is extracted from the custom MUTEX and is in an analogue form. Thus the need to design a tool to convert from analogue to digital value is obvious. This is achieved by setting a threshold value and digitizing the data into zero and ones. When this process of data has been made the result is a set of data to graph. Also the need to simulate the response of the circuit under variability conditions inserts the need of a tool that affects the circuit with time-zero variability. The purpose of the design of an automated system is it's use in a unified simulation environment without the need of manually extracting data from files. Also it gives the possibility of adjustments in various parameters of the system, such as the resolution of the sensor.

In this thesis the environment of Matlab is used in order to built this automated system. With the use of scripts and tools written in a programming language, either C++ or Perl we have the production of reliability curves and estimations. The scripts make use of the tools designed to parse data and then use them to produce the targeted curve. As shows in the following sections curves such as Monte Carlo and Yield curves are produced in order to have a complete view of the sensors response under time-zero variability conditions.

4.2 Simulation Set-up

In figure 4.1 is presented a flowchart of the simulation set-up. There are two main domains, the Yield analysis and the Monte Carlo analysis which are going to be explained in the next paragraphs.

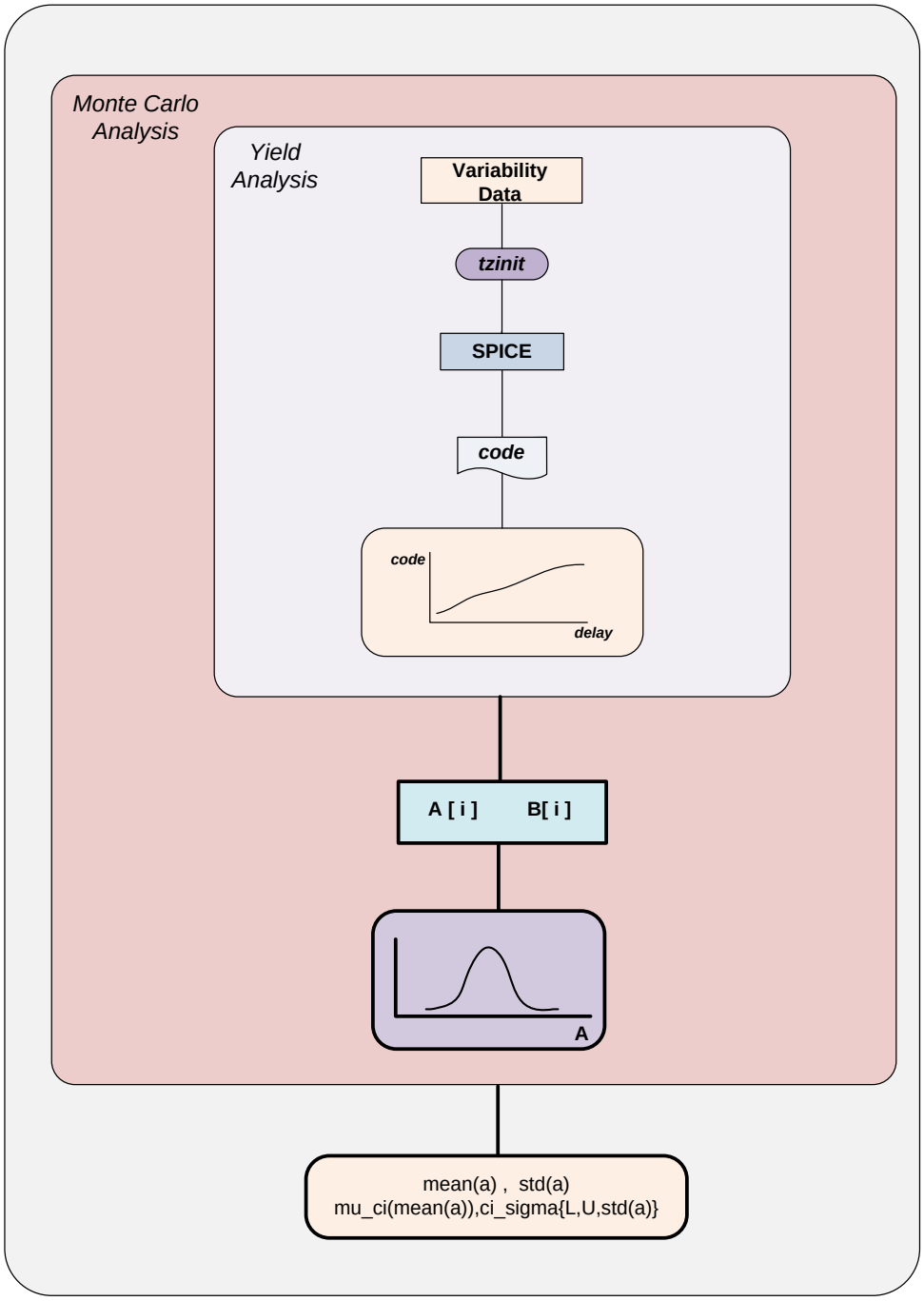


Figure 4.1: Flowchart of Yield Analysis

4.3 Yield Analysis

According to the previously mentioned theory the first step on observing a sensor's response in an environment with variations is it's design following the TDIM. In the simulation tool, `ngspice`, the design of each sensor is done on two levels, the front-end design named *netlist.cir* and the *subcircuit* file which contains the detailed circuit. In the *subcircuit*'s level each logic gate, mutex and especially each cell has been described with the sizing of the transistors following the fractions we mentioned in paragraphs 3.2 and 3.3. The front-end file contains the number of the input and outputs of the monitor and also defines the inserted pulses. As seen later due to the need of a varying relative delay between the two inputs this part is made customizable.

The technology of the implementation is chosen from the imported *modelcard*. The model card included in the *netlist.cir* is the model BSIM4v5 [29] and 'it addresses the MOSFET physical effects into sub-100nm regime'.

As figure 4.2 shows, after the completion of the design of the sensor, Spice simulation sequences. The result of this simulation is automatically saved in a file named *output* where all the information of the voltages and time are in a non-readable format. In the view of an automated system this file is parsed by a tool written in C++, the *Postprocessor*.

Postprocessor accesses the *output* file and extracts the information of the number of outputs the circuit has. This advantage makes the system capable of handling information of circuits with varying number of outputs. Thus to change the monitors resolution is a customization easily made by adding or extracting cells from the spice files. So if we want to increase the robustness of the sensor under investigation we can add cells and then start the testing with the same system.

The result of the run of *postprocessor* is the production of individual files that include the data of every output of the circuit. Through these files it is made possible to plot the detailed response of the sensor and extract the graphs seen in paragraphs 3.2 and 3.3. From these readable data of the output of each cell this tool also converts the analogue values to a compact digital code. This is achieved by setting a threshold value and comparing every analogue value with it. As previous discussed the digital code has as many digits as the

number of the cells.

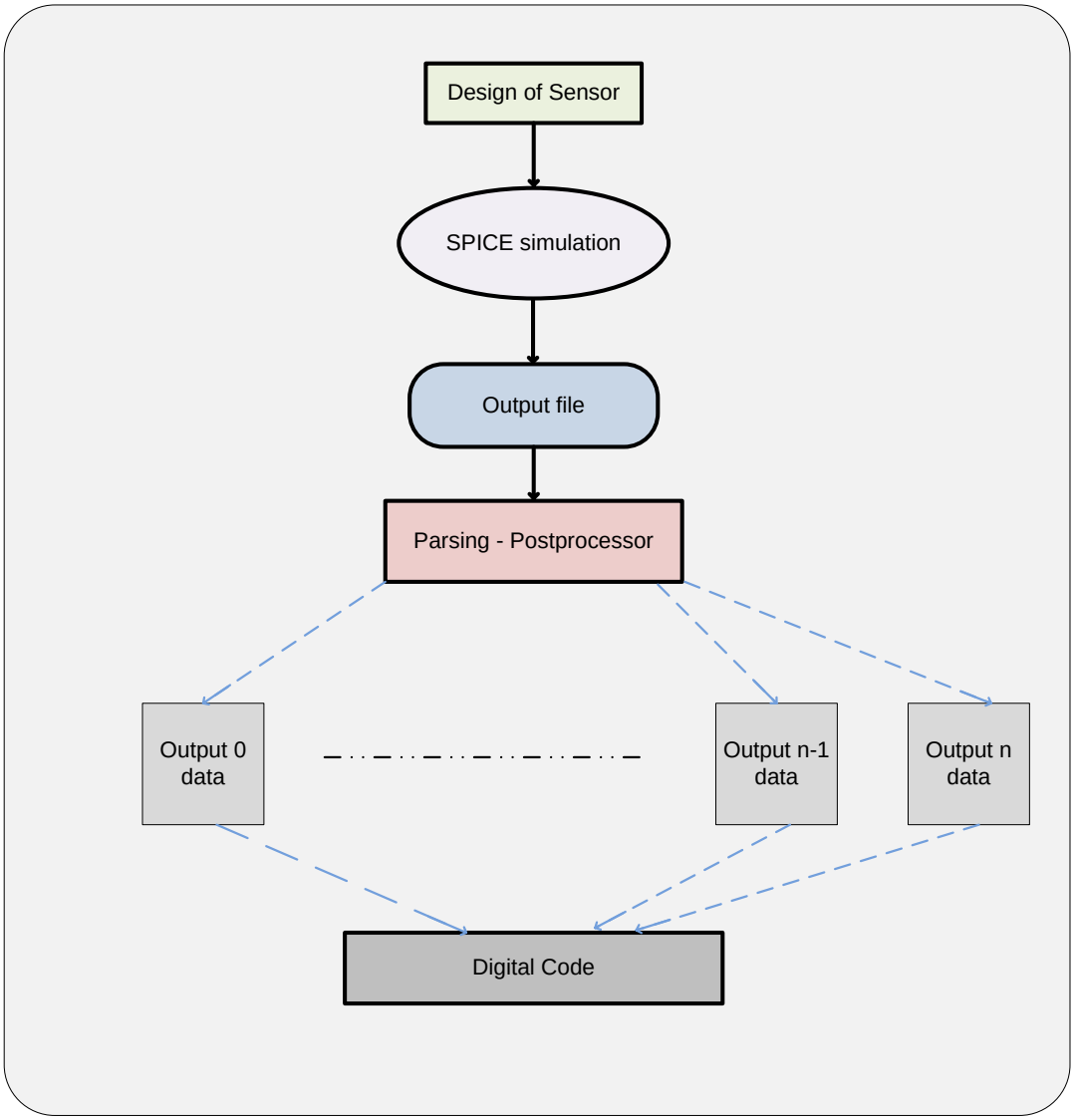


Figure 4.2: Conversion of Simulation Data Flowchart

For a complete yield analysis the sensor under investigation must be simulated under variability and non-variability environment conditions. In order to have a stand-alone tool that will produce the yield curves of each sensor we have designed a Matlab script which

automatically calls a number of tools in order to have a Monte Carlo session with varying input parameters. Specifically the data for a curve without the time-zero variability can be collected by running the simulation explained in the previous section.

With the use of a sub-tool *inputmaker* which is designed to access the file with the data of the input pulses, the Matlab script varies in a linear space step the time difference between them. As the *postprocessor* tool extracts and saves the digital code of each simulation in a file the data can be easily plotted.

The 'Design of Sensor' shown in Figure 4.2, with the ability of linearly increasing the time difference between the two signals inserted, is shown in Figure 4.3 as Spice Design and includes the sub-tool *inputmaker*.

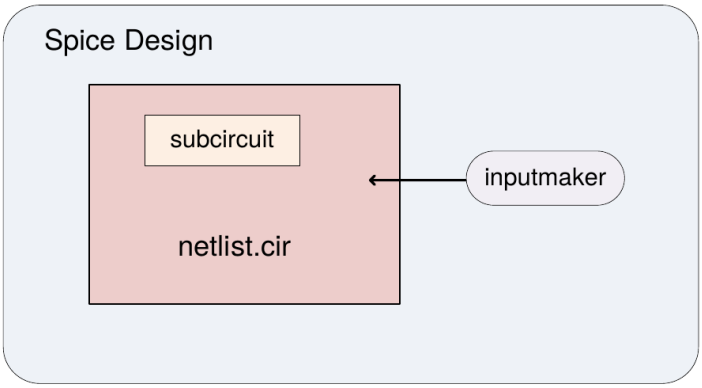


Figure 4.3: Conversion of Simulation Data Flowchart

To have a yield estimation we make use of the tool *tzinit* [30] which initialize the time-zero variables, such as the threshold voltage (Vth_0) of the device. This function of this tool is an equivalent of time-zero variability and inserts the yield factor in our system.

As shown in the figure 4.1 this time-zero initialization is applied before every Spice simulation and the data extracted are influenced. The yield plots need to have the reference curve which is without the time-zero variability and the curve which will characterize the deviation from the reference because of the variability in the system.

In conclusion the final form of the script *yield.m* consists of the specification of the time difference of the two inputs and two loops which simulate the testing of the sensor with and without time-zero variability. It is expected the curve with the yield factor to have a

profound slope to the reference curve which characterize the sensor with no aging factors.

4.4 Monte Carlo Analysis

When proposing a design of an aging sensor it is advisable to include a validation of the sensors response, which automatically suggests the production of a Monte Carlo Curve. To have a complete reliability estimation of the two sensors designed according to the TDIM we have also examined their responses under repetitive simulations.

It is impossible and infeasible for a circuit to be measured and extract a specific value of response. To obtain a probability distribution of samples of a circuit is called Monte Carlo analysis. This random sampling is expected to act as a Gaussian Curve and have a mean value (μ) that most of the values have greater possibility to be near it. As mentioned in a previous section 2.5, to characterize a system's behaviour we have to estimate a mean value of measurements and a standard deviation from this value.

The Monte Carlo Analysis is produced by a Matlab script which contains part of the yield analysis mentioned before, as shown in figure 4.1. Specifically from the credibility curves produced by the yield analysis of the two sensors implemented, we gather the A and B values which are the coefficients of the polynomial that characterizes the curve.

By plotting a histogram of the values A and B we can have an estimation on the standard deviation (σ) and the mean value (μ) of the circuit under investigation. The precision of these estimations is based on the repetitions of the simulation. A relative large number of iterations is selected, i.e. 150, to extract a reliable normal distribution of the two sensors. If choosing to run less times the simulation process, the distribution is not so accurate but by selecting to increase the repetitions the simulation grows too slow.

From the curves produced we are able to calculate the mean value and the standard deviation for the sensor for on-chip measurements and the sensor for the automotive applications. The Matlab script which is responsible for the Monte Carlo analysis makes use of two sub-tools which represent the formulas for the mean value and the standard deviation.

After the Monte Carlo simulation of 150 runs for each sensor, from the Gaussian distribution with $\pm 3\sigma$ variation we can extract the mean and the standard deviation of the

circuit under test. We can also evaluate the upper and lower limits of each metric with 95% confidence interval for the reliability estimated from the proposed modes using various samples of checkpoints. The 5% is the percentage that a new observation will fall out of the bounds.

As seen in the flowchart figure 4.1 to run the simulation that will result in the production of the Confidence Interval of each sensor includes the Monte Carlo simulation in order to gather the data and calculate the standard deviation and mean value of the sensor. The accuracy of the estimated μ andσ is directly linked with the number of iteration the Monte Carlo simulation runs. Thus this experiment consists of a variable which starts from a minimum value of iteration and increases to a respective number in order to have a credible result.

The information extracted from a Confidence plot is the minimum threshold of iteration that can be used in a simulation to have credible conclusions. By calculating and plotting the deviation from the mean value in each number of iterations results also in having an estimation on the reliability of each circuit that is being simulated.

Chapter 5

Verification Tests and Results

5.1 Introduction

In this Chapter we will include the results of the simulations that are thoroughly explained in Chapter 4. Purpose of the sections following is to discuss the plots of each separate analysis and compare them with the expected results according to the background theory. Through that we can observe any behaviour which deviates the expected and have an estimation of the sensors response under conditions of time-zero variability.

The experimental analysis which is explained in paragraphs 4.3 to 4.4 is applied in two aging sensors implemented in `ngspice`. The Time Delay Interpolation Method is the philosophy behind designing and also testing these sensor. The results following, concerning the two sensors described in Chapter 3, are Yield Analysis, Monte Carlo Analysis, Confidence Intervals and a Voltage Sweep Test.

The data extracted from the experiments are automatically imported in Matlab and from there are handled and plotted in the graphs presented in the next paragraphs. From this integrated analysis we can have a reliable estimation on the sensors performance and reliability in an environment with time-zero variability.

5.2 Monte Carlo Analysis

The two sensors implemented are used as TDCs and convert the interpolation of the input pulses to digital code. This is shown in the two figures 5.1, 5.2 which are the responses for a varying initial time delay for the first and the second sensor, respectively. The two curves included represent the circuit's response with and without the effect of time-zero variability.

The slope and the intercept of the line with time-zero variability for each sensor are referred as the A and B values and are gathered through repeating the simulation for the Monte Carlo analysis. The expected output of this test is a linear response, meaning every digital code to represent the initial time difference between the pulses inserted

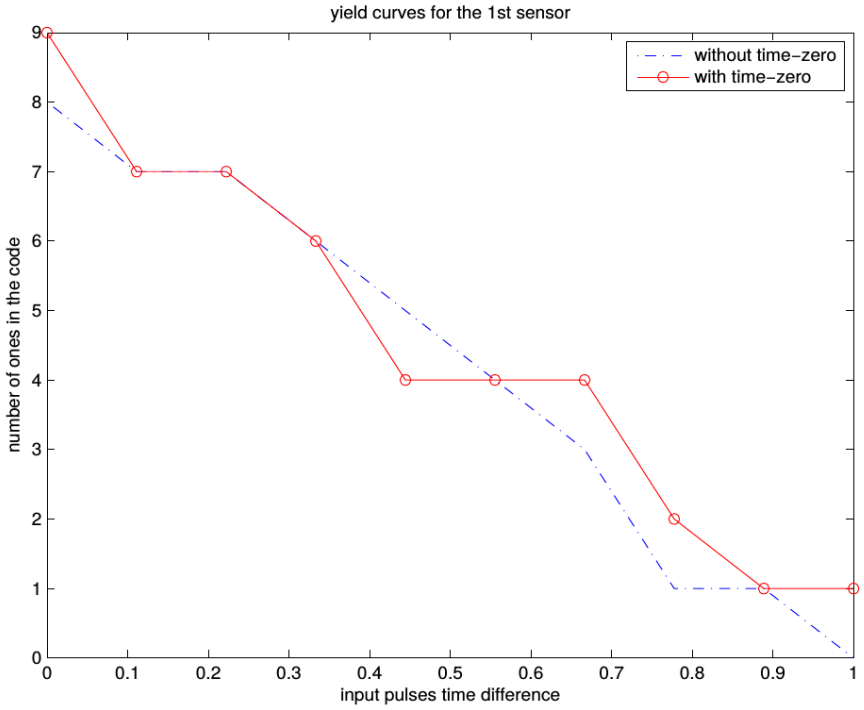


Figure 5.1: Time to digital code 1st sensor

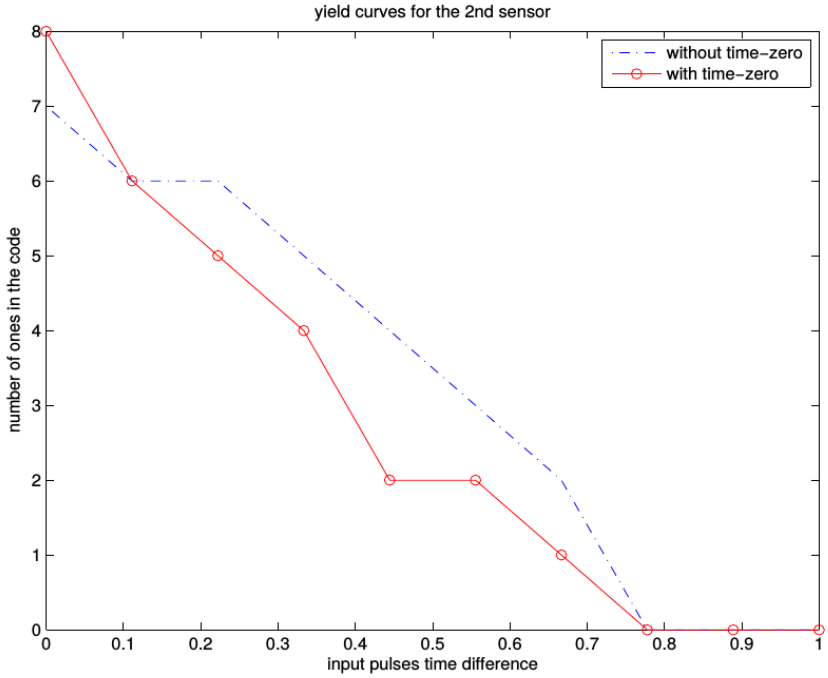


Figure 5.2: Time to digital code 2nd sensor

As mentioned in the Section 4.4, a standard deviation graph is usually produced when simulating the response of a circuit, meaning that it's response is going to vary around a mean value and most of the results are going to be near the mu.

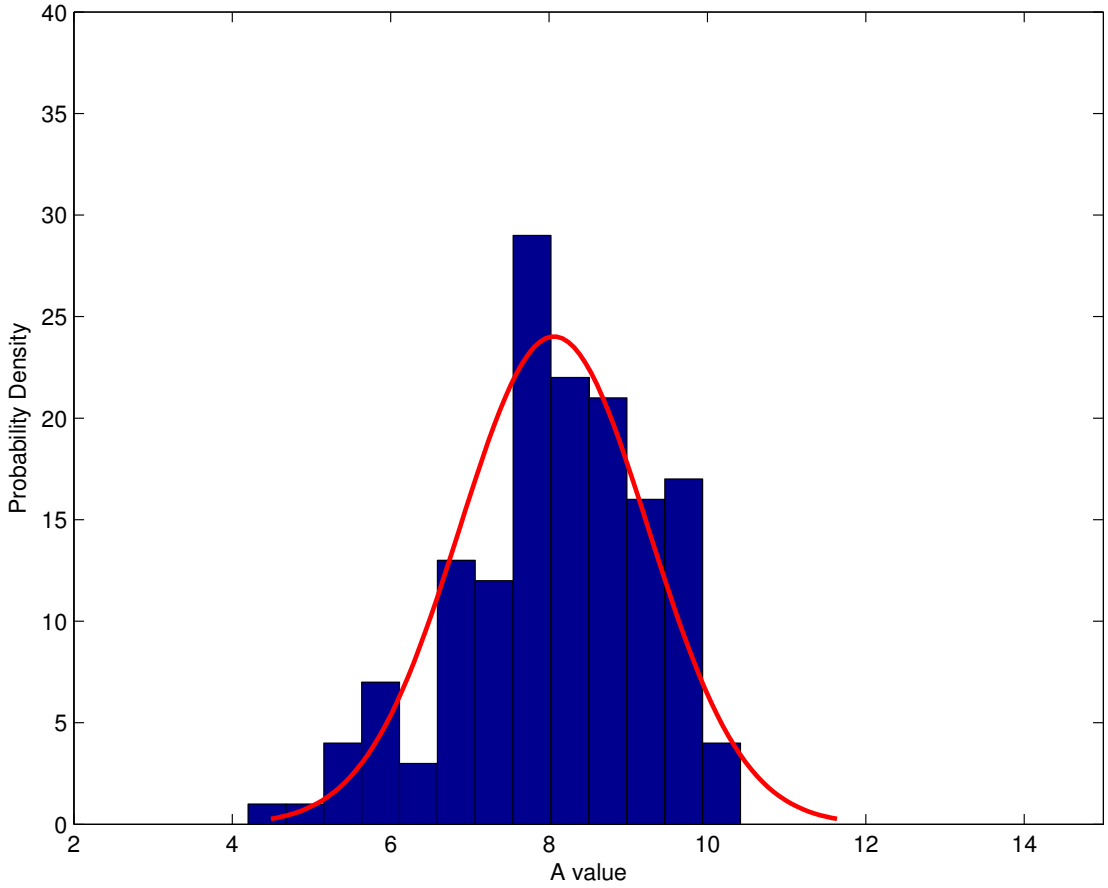
The figures presented, 5.3, are produced from the Monte Carlo (MC) simulation of the two sensors. The iterations of the experiment are set in 150, in order to extract a reliable normal distribution. If choosing to run less times the simulation process, the distribution is not so accurate. We have made this compromise in the accuracy vs the time that the experiments need, and chose a big number of iterations. This is not so perceptible in the MC analysis but in the simulations following which include many MC iterations the time needed increases exponentially.

From the histograms following we are able to calculate the mean value and the standard deviation for the sensor for on-chip measurements and the sensor for the automotive applications. For this procedure there are used two tools written in Perl which are called from the Matlab script.

The first figure of 5.3 represents the distribution of A value which is, as mentioned before,

the coefficient of the yield curve. The second figure shows the distribution of B value of the first sensor. We observe that the distribution is of 2-sigma yield with 95% confidence. This shows the yield of the sensors. To have a 3-sigma yield there is the obvious need to take over 1000 samples. The circuits fail to hit the targeted yield and it can be said that their actual yield is very poor.

The same method for the production of MC analysis for the second sensor produces the following figures. The first, 5.4 represents the distribution of A values, whereas 5.4 shows the B values, both for 150 iterations. It can be observed that although the samples are over 100 the circuits does not hit the 2-sigma yield.



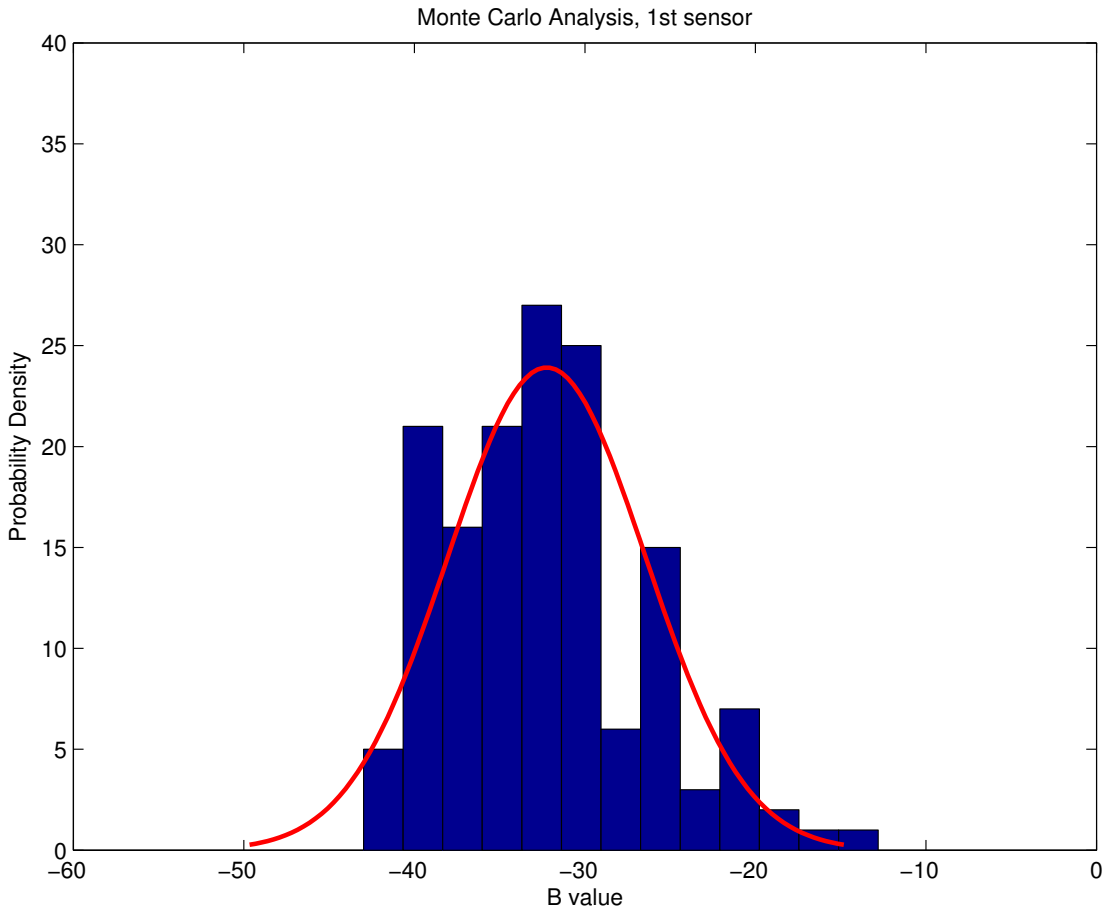
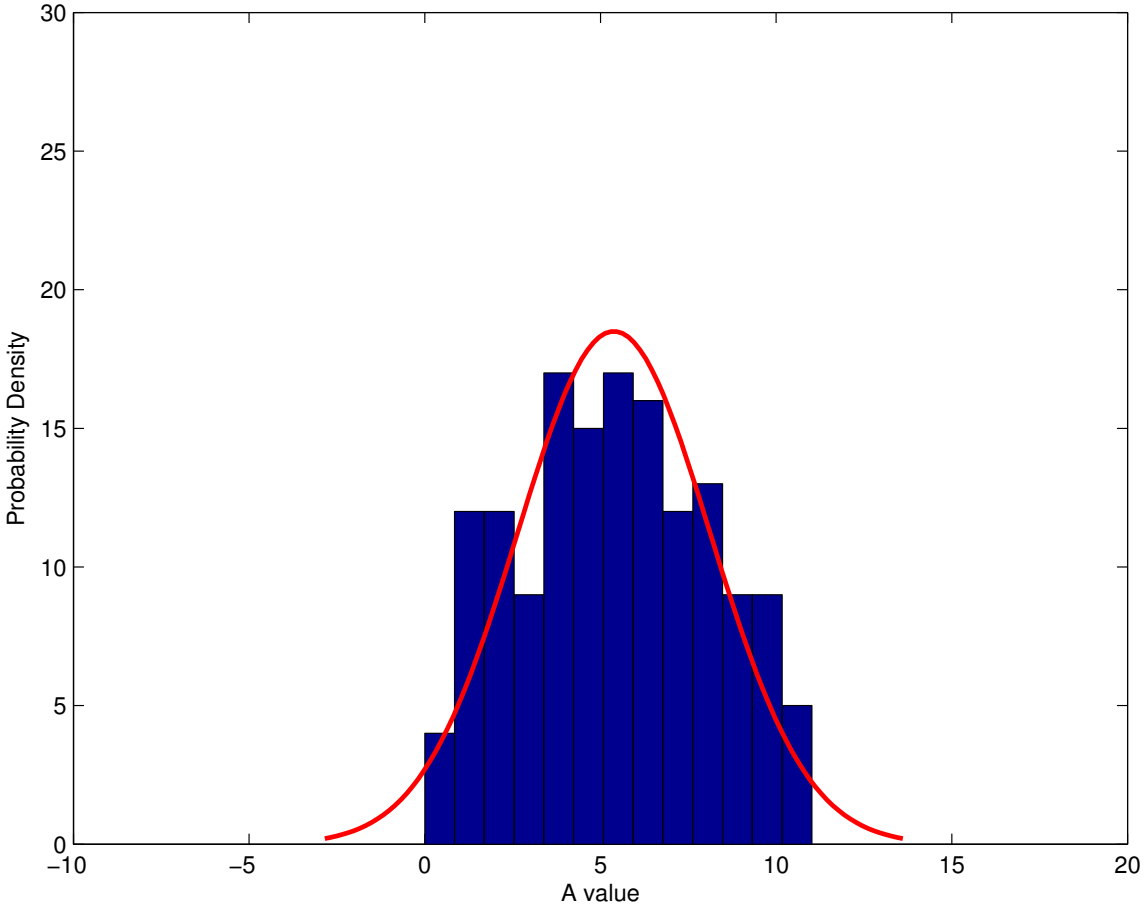


Figure 5.3: Monte Carlo Analysis, 1st sensor



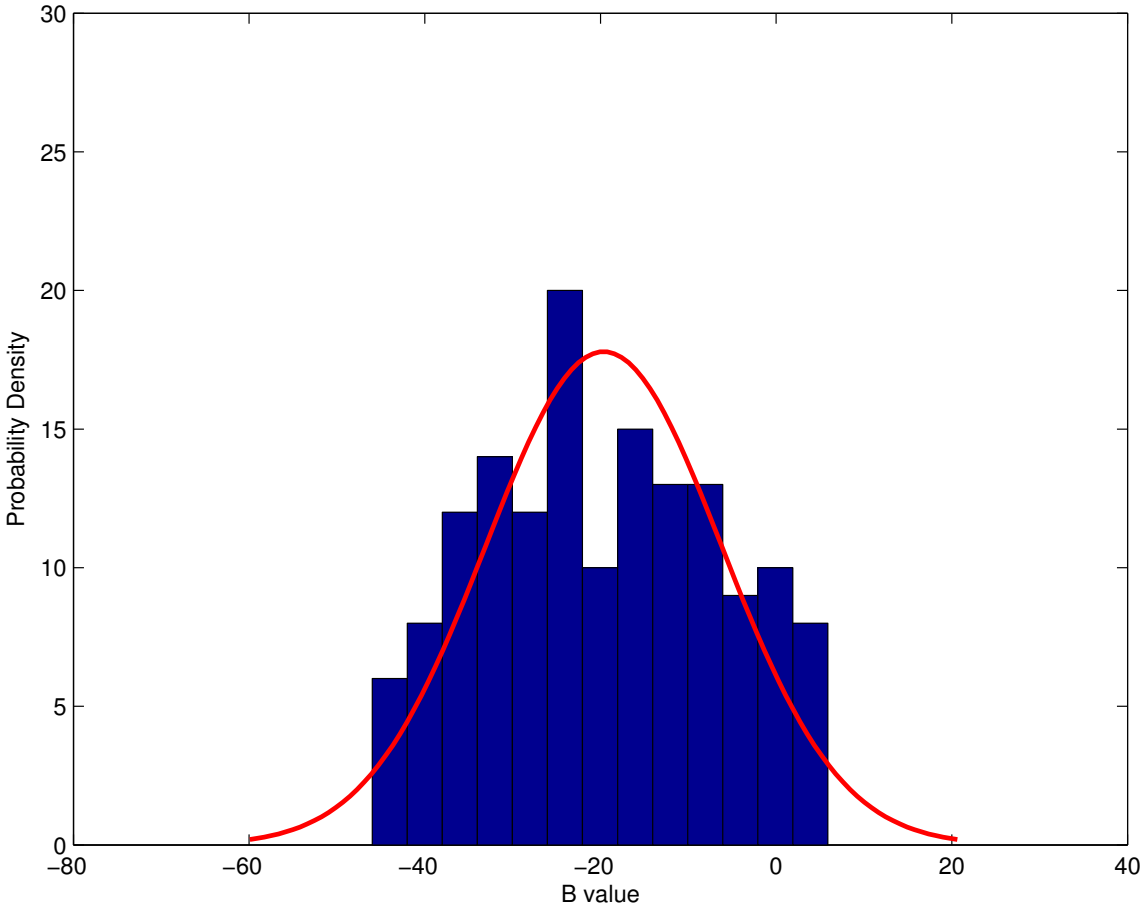


Figure 5.4: Monte Carlo Analysis, 2nd sensor

5.3 Execution Time versus Accuracy

After the MC analysis for each sensor, follows the production of Confidence Intervals (CI). From the Gaussian distribution with $\pm 3\sigma$ variation we extract the μ and σ of the circuit under test. We also evaluate the upper and lower limits of each metric with 95% confidence interval for the reliability estimated from the proposed modes using various samples of checkpoints.

In figure 5.5 and 5.6 we see the Confidence Intervals for the two sensors, from which we can obtain an estimation of the variations of the values in each number of iterations. In the two figures are plotted the upper and lower confidence limits of both mean and standard deviation.

It is obvious that when taking more samples the CI will be tightened up. We can observe that the precision of the measured mean value or standard deviation is determined by the number of iterations. When selecting to run a Monte Carlo simulation with less than 100 iterations this analysis is prone to errors and should not be considered valid.

Although Confidence interval tend to be narrower and closer to true reliability when the simulation increases the number of runs, we can see that the upper and lower limits stay the same from the checkpoint of 120 iterations. This depends on the yield of the sensor.

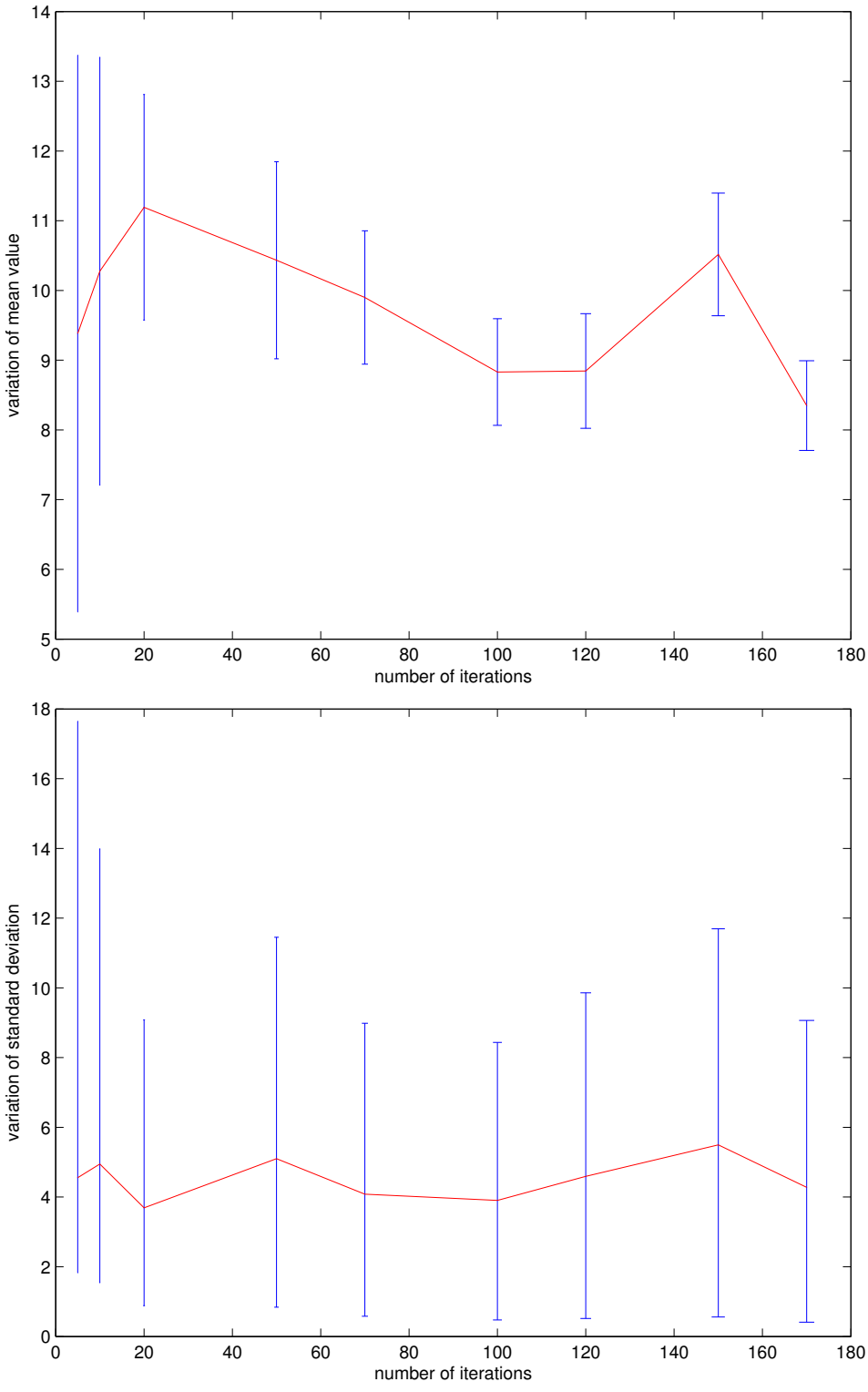


Figure 5.5: Confidence Interval of the First Sensor

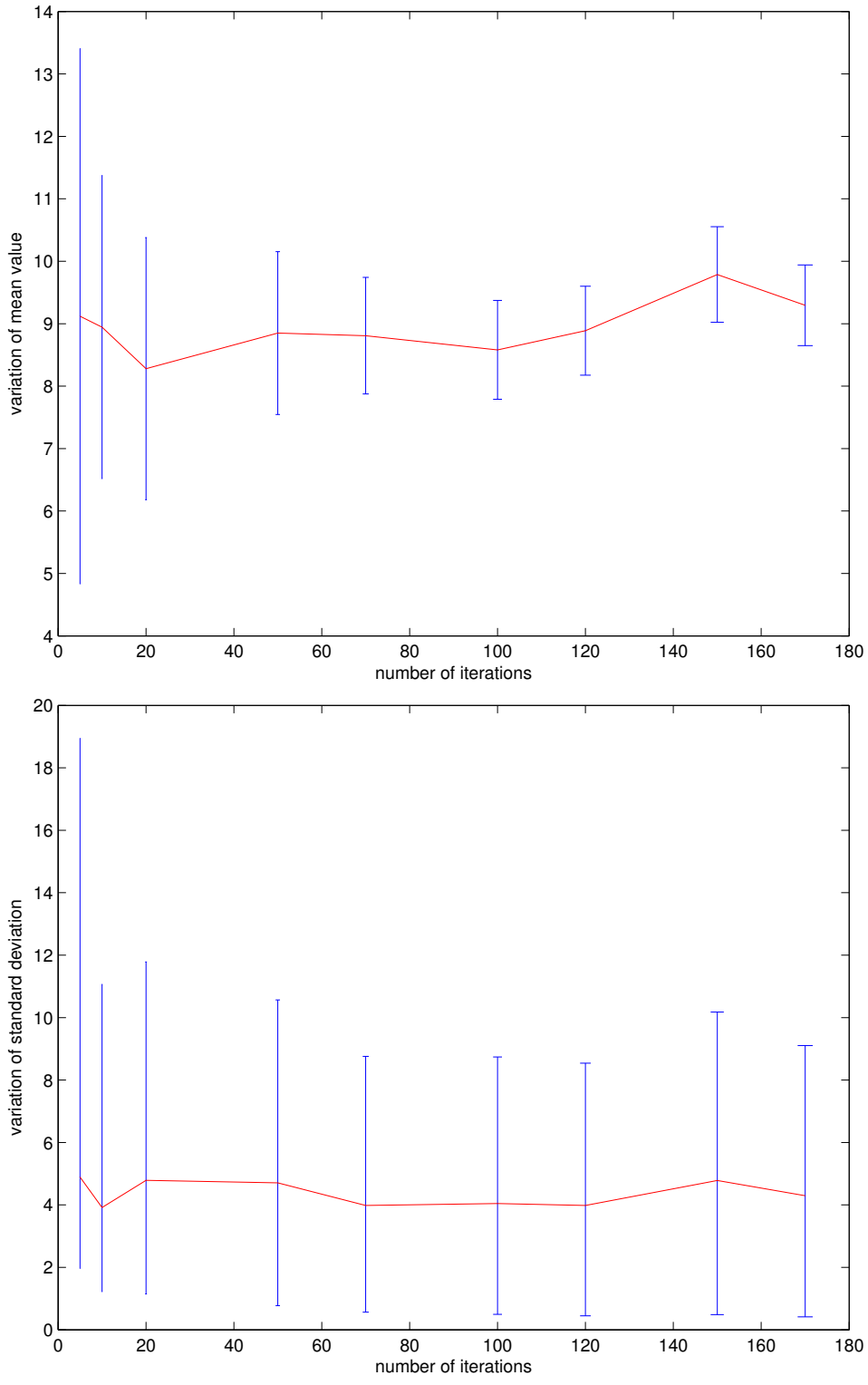


Figure 5.6: Confidence Interval of the Second Sensor

5.4 Voltage Sweep Test

As shown in figure 4.1 we calculate each mean and standard deviation value from each Gaussian Curve formed from `ngspice` simulation 5.3, 5.4. The iterations of MC simulations are set in 150 to have a good estimation of the values produced. For plotting the characteristic sensitivity surface we have to keep track of the mean and σ values of A and B which are the polynomial factors of the yield curve for varying standard deviation either of p or nMOS transistors and the logarithmic increase of the standard deviation for both p and nMOS.

When we artificially vary the standard deviation in an environment with time-zero variability we can observe the response of the sensor and have an estimation on the reliability of the metrics according to an initial measurement. The reference points are measured with the initial value of σ. The next values of σ are calculated by multiplying the absolute value of the threshold voltage in time-zero with a variable which increases in logarithmic step.

In the following figures there is a three dimensional representation of the mean values of A and B for both p and nMOS transistors in a varying standard deviation environment. For a better understanding there is also a two dimensional representation as seen the surface from above. In figures 5.8 and 5.10 there is an arrow which shows the reference value of the metrics of the system.

It is obvious that by sweeping the threshold voltage by little the deviation from the initial value is great, thus the sensors show no resilience to variations and can not be considered reliable in harsh environments.

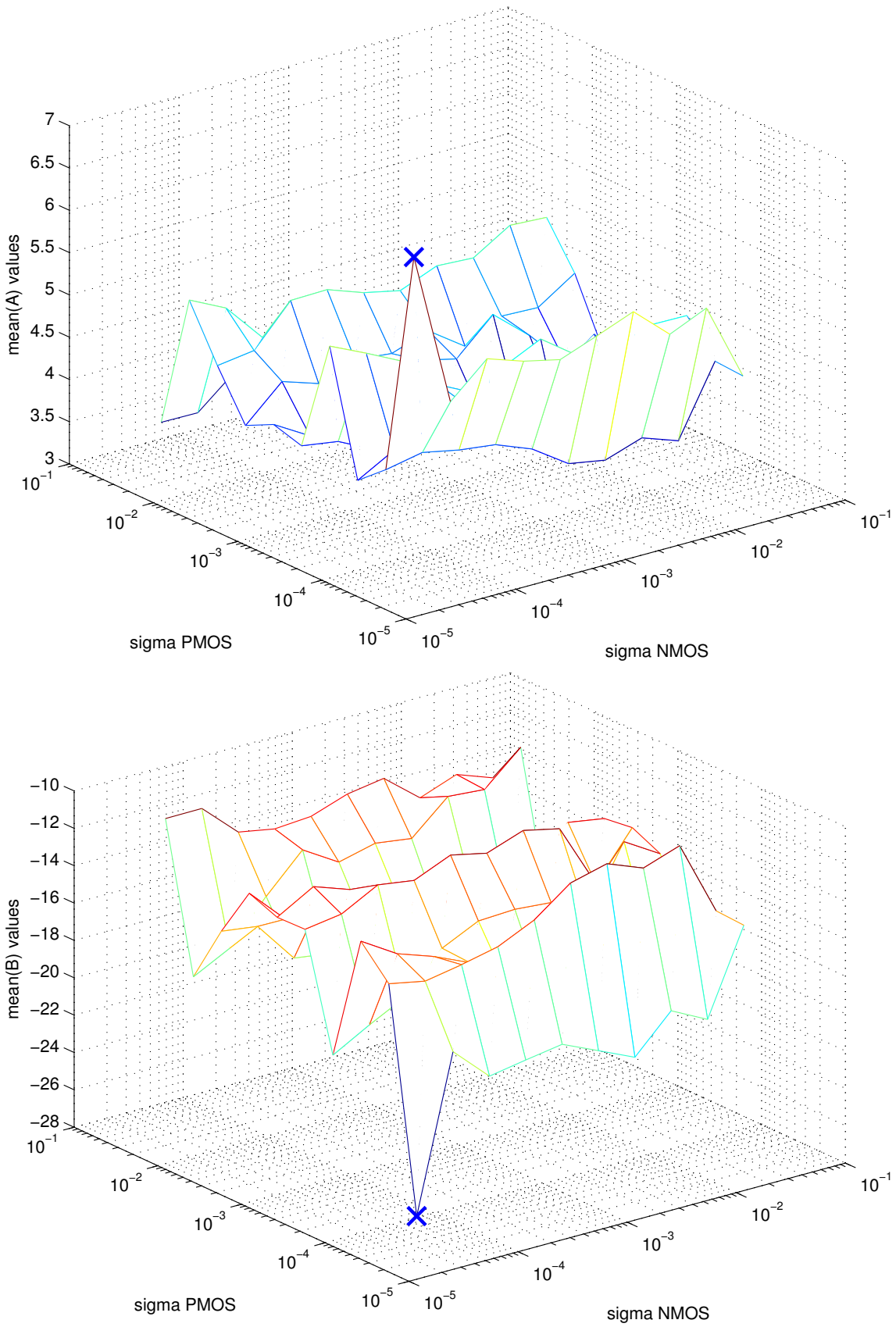


Figure 5.7: Voltage Sweep Test, 1st sensor

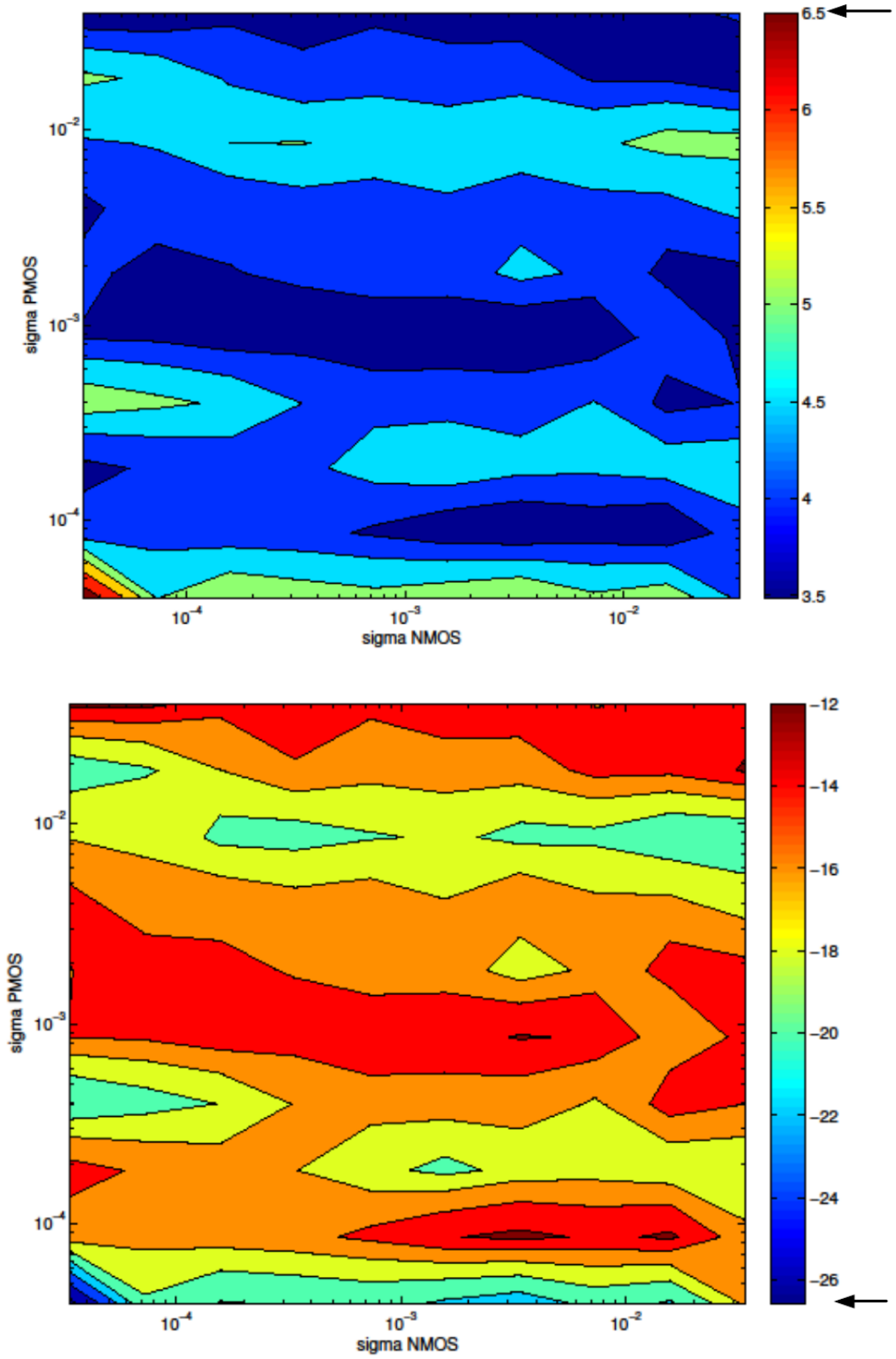


Figure 5.8: Voltage Sweep Test, 1st sensor

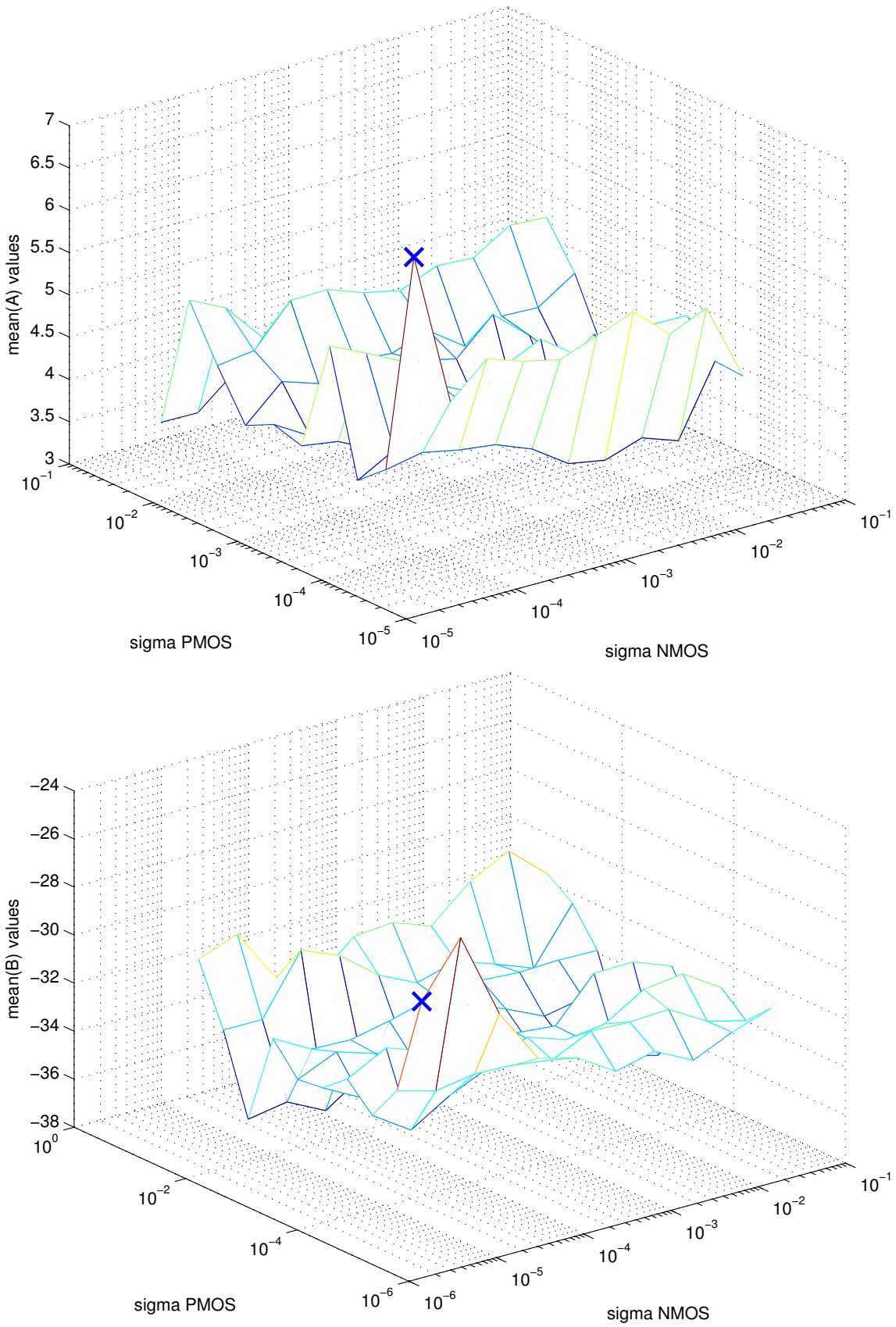


Figure 5.9: Voltage Sweep Test, 2nd sensor

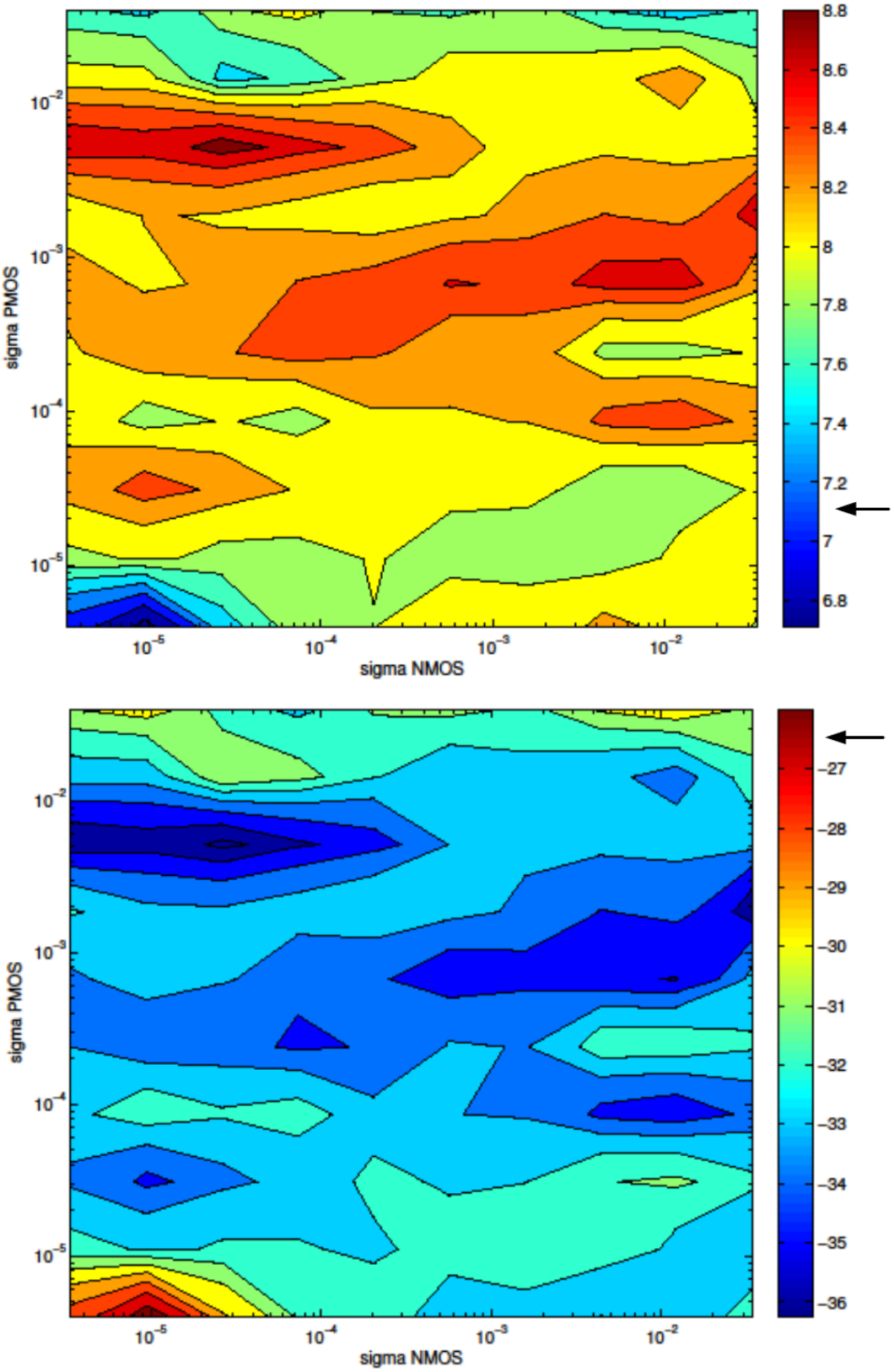


Figure 5.10: Voltage Sweep Test, 2nd sensor

Chapter 6

Conclusions

Although embedded sensors and specifically TDCs are an important part for monitoring and testing a circuit, they are not followed with a complete reliability profile. There should be a extensive procedure of testing and production of credibility metrics for each sensor proposed. As seen in this thesis the two sensors that were under investigation do not respond credibly under Time-zero variability. To have though a complete model of variability, there should be the introduction of time-dependent variabilities. Under the combination of these variation parameters one could have a more reliable estimation of the yield and the credibility profile of the two sensors.

Through the MC analysis and the production of credibility curves the results where that there is an obvious need of exceeding the hundreds of iterations in the simulations. This is infeasible for the length of this experiment but is crucial in order to have a credible set of responses. Another observation made through this thesis is that there is not a global number of the MC iterations, but if you intent to the production of a Gaussian curve you must choose more than 100 iterations on the experiment.

When designing the experiment for testing the sensor, the importance of selecting the iterations is great as it immediately impacts on the simulation time. In the voltage sweep test we observed that the selection of MC iterations plays the most important role compared to the number of the times the experiment is conducted, as it affects the precision of the measurements. The number of 150 iterations is already a good approximation for the MC

analysis and by increasing it, it will result in time cost and won't improve the results in an observable point.

To meet real aging criteria of the modern circuits there is the need of a realistic model of time-zero variability and also introduction in the testing process of time-dependent variations. The need of better and more accurate phenomenon representation is obvious and should concern the future work in the section of reliability.

According to a Pelgrom's plot the σ of the threshold voltage of two, or more devices, can vary although they may have the same sizing. It also supports that when increasing the sizing of FETs the σ of the V_{th} increases accordingly. This has not taken into account through this thesis and the Pelgrom's law has not been introduced into the σ estimation of our experiments. If the law was taken into account it would make more realistic delay monitor characterization. Another factor that Pelgrom's law suggests is to take under consideration the sizing of the transistors. Given the law we could up-size the monitors and increase their credibility.

A final observation is that the flow design in this thesis is scalable, which means that the number of simulations is independent from the size of the circuit. One can reduce the simulation time by selecting less number of cells, although this would decrease the accuracy of the delay measurements of the monitors. Thus one should decide the trade-off between speed and accuracy through selecting also the number of iterations. The drawback of this flaw is the introduction of only time-zero variations, and not taking under consideration the process variation, which is a dominant factor in circuits, but by simulating two different sensor topologies it is shown that it could simulate every other sensor based on Time Delay interpolation method.

References

[1] M. A. Abas, G. Russell, and D. Kinniment, "Design of sub-10-picoseconds on-chip time measurement circuit," in *Proceedings of the conference on Design, automation and test in Europe-Volume 2*, p. 20804, IEEE Computer Society, 2004.

[2] J. C. Vazquez, V. Champac, I. C. Teixeira, M. B. Santos, and J. P. Teixeira, "Programmable aging sensor for automotive safety-critical applications," in *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2010*, pp. 618–621, IEEE, 2010.

[3] B. Kaczer, S. Mahato, V. V. de Almeida Camargo, M. Toledano-Luque, P. J. Roussel, T. Grasser, F. Catthoor, P. Dobrovolny, P. Zuber, G. Wirth, *et al.*, "Atomistic approach to variability of bias-temperature instability in circuit simulations," in *Reliability Physics Symposium (IRPS), 2011 IEEE International*, pp. XT–3, IEEE, 2011.

[4] M. Toledano-Luque, B. Kaczer, J. Franco, P. J. Roussel, T. Grasser, T. Y. Hoffmann, and G. Groeseneken, "From mean values to distributions of bti lifetime of deeply scaled fets through atomistic understanding of the degradation," in *IEEE VLSI Technology Symposium Tech Dig*, pp. 152–153, 2011.

[5] G. Kornaros and D. Pnevmatikatos, "A survey and taxonomy of on-chip monitoring of multicore systems-on-chip," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 18, no. 2, p. 17, 2013.

[6] T. McConaghy and J. Hogan, *Variation-Aware Design of Custom Integrated Circuits: A Hands-on Field Guide*. Springer, 2013.

[7] R. R. Schaller, "Moore's law: past, present and future," *Spectrum, IEEE*, vol. 34, no. 6, pp. 52–59, 1997.

[8] D. K. Schroder and J. A. Babcock, "Negative bias temperature instability: Road to cross in deep submicron silicon semiconductor manufacturing," *Journal of Applied Physics*, vol. 94, no. 1, pp. 1–18, 2003.

[9] A. Kerber, E. Cartier, L. Pantisano, M. Rosmeulen, R. Degraeve, T. Kauerauf, G. Groeseneken, H. Maes, and U. Schwalke, "Characterization of the v t-instability in sio 2/hfo 2 gate dielectrics," in *Reliability Physics Symposium Proceedings, 2003. 41st Annual. 2003 IEEE International*, pp. 41–45, IEEE, 2003.

[10] B. Kaczer, T. Grasser, P. J. Roussel, J. Franco, R. Degraeve, L.-A. Ragnarsson, E. Simoen, G. Groeseneken, and H. Reisinger, "Origin of nbti variability in deeply scaled pfets," in *Reliability Physics Symposium (IRPS), 2010 IEEE International*, pp. 26–32, IEEE, 2010.

[11] G. I. Wirth, J. Koh, R. da Silva, R. Thewes, and R. Brederlow, "Modeling of statistical low-frequency noise of deep-submicrometer mosfets," *Electron Devices, IEEE Transactions on*, vol. 52, no. 7, pp. 1576–1588, 2005.

[12] Z. Chen, K. Hess, J. Lee, J. W. Lyding, E. Rosenbaum, I. Kizilyalli, S. Chetlur, and R. Huang, "On the mechanism for interface trap generation in mos transistors due to channel hot carrier stressing," *Electron Device Letters, IEEE*, vol. 21, no. 1, pp. 24–26, 2000.

[13] J. Franco, B. Kaczer, M. Toledano-Luque, P. J. Roussel, B. Schwarz, M. Bina, M. Waltl, T. Grasser, and G. Groeseneken, "Reduction of the bti time-dependent variability in nanoscaled mosfets by body bias," in *IEEE Proceedings of International Reliability Physics Symposium (IRPS)*, 2013.

[14] A. Asenov, S. Roy, R. Brown, G. Roy, C. Alexander, C. Riddet, C. Millar, B. Cheng, A. Martinez, N. Seoane, *et al.*, "Advanced simulation of statistical variability and relia-

bility in nano cmos transistors," in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, pp. 1–1, IEEE, 2008.

[15] A. Asenov, S. Kaya, and A. R. Brown, "Intrinsic parameter fluctuations in decananometer mosfets introduced by gate line edge roughness," *Electron Devices, IEEE Transactions on*, vol. 50, no. 5, pp. 1254–1260, 2003.

[16] A. Gu and A. Zakhor, "Optical proximity correction with linear regression," *Semiconductor Manufacturing, IEEE Transactions on*, vol. 21, no. 2, pp. 263–271, 2008.

[17] M. J. Pelgrom, A. C. Duinmaijer, A. P. Welbers, *et al.*, "Matching properties of mos transistors," *IEEE Journal of solid-state circuits*, vol. 24, no. 5, pp. 1433–1439, 1989.

[18] B. Kaczer, M. Toledano-Luque, J. Franco, and P. Weckx, "Statistical distribution of defect parameters," in *Bias Temperature Instability for Devices and Circuits*, pp. 161–176, Springer, 2014.

[19] S. Mangan, A. Zaslaver, and U. Alon, "The coherent feedforward loop serves as a sign-sensitive delay element in transcription networks," *Journal of molecular biology*, vol. 334, no. 2, pp. 197–204, 2003.

[20] M. Maymandi-Nejad and M. Sachdev, "A digitally programmable delay element: design and analysis," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 11, no. 5, pp. 871–878, 2003.

[21] J. Kalisz, "Review of methods for time interval measurements with picosecond resolution," *Metrologia*, vol. 41, no. 1, p. 17, 2004.

[22] S. Henzler, S. Koeppe, D. Lorenz, W. Kamp, R. Kuenemund, and D. Schmitt-Landsiedel, "A local passive time interpolation concept for variation-tolerant high-resolution time-to-digital conversion," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 7, pp. 1666–1676, 2008.

[23] J.-P. Jansson, A. Mantyniemi, and J. Kostamovaara, "A cmos time-to-digital converter with better than 10 ps single-shot precision," *Solid-State Circuits, IEEE Journal of*, vol. 41, no. 6, pp. 1286–1296, 2006.

[24] R. B. Staszewski, S. Vemulapalli, P. Vallur, J. Wallberg, and P. T. Balsara, "1.3 v 20 ps time-to-digital converter for frequency synthesis in 90-nm cmos," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 53, no. 3, pp. 220–224, 2006.

[25] A. Mantyniemi, T. Rahkonen, and J. Kostamovaara, "A cmos time-to-digital converter (tdc) based on a cyclic time domain successive approximation interpolation method," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 11, pp. 3067–3078, 2009.

[26] J. Benesty, J. Chen, and Y. Huang, "Time-delay estimation via linear interpolation and cross correlation," *Speech and Audio Processing, IEEE Transactions on*, vol. 12, no. 5, pp. 509–519, 2004.

[27] S. D. Brown and Z. G. Vranesic, *Fundamentals of digital logic with VHDL design*, vol. 70125910. McGraw-Hill New York, 2000.

[28] V. Agrawal, "Implementation of bist structure using vhdl for vlsi circuits,"

[29] P. Nenzi and H. Vogt, *Ngspice Users Manual*, January 2013.

[30] D. Rodopoulos, P. Weckx, M. Noltsis, F. Catthoor, and D. Soudris, "Atomistic pseudo-transient bti simulation with inherent workload memory," *Device and Materials Reliability, IEEE Transactions on*, vol. 14, pp. 704–714, June 2014.